IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., Plaintiff, v. FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., and FAIRCHILD SEMICONDUCTOR CORPORATION, Defendants.	)	C.A. No. 04-1371-JJF

STIPULATION PERMITTING DEFENDANTS TO FILE AN AMENDED ANSWER

WHEREAS Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corp. (collectively "Fairchild") wish to file an Amended Answer in the form attached hereto as Exhibit A;

WHEREAS the parties agree that Fairchild's Amended Answer will not require additional discovery and will not serve as a basis for Fairchild to seek an extension to either the trial date or the case schedule; and,

WHEREAS Plaintiff Power Integrations, Inc. ("Power Integrations") does not agree with the assertions of inequitable conduct or the characterizations of events in the new matter in Fairchild's Amended Answer, but Power Integrations does not oppose Fairchild's filing of its Amended Answer,

NOW THEREFORE THE PARTIES AGREE to permit Fairchild to file the Amended Answer attached hereto as Exhibit A.

FISH & RICHARDSON, P.C.

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DEFENDANTS FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC. AND FAIRCHILD SEMICONDUCTOR CORPORATION'S FIRST AMENDED ANSWER AND COUNTERCLAIMS TO PLAINTIFF'S FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT AND DEMAND FOR JURY TRIAL

Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation (collectively "FAIRCHILD") answer the First Amended Complaint of Power Integrations, Inc. ("PI") as follows:

FAIRCHILD denies each and every allegation contained in the First Amended Complaint, except as hereinafter specifically admitted or explained. To the extent that the headings, or any other non-numbered statements in Plaintiff's First Amended Complaint contain any allegations, Defendants deny each and every allegation therein.

THE PARTIES

1. In response to paragraph 1 of the First Amended Complaint, FAIRCHILD lacks sufficient knowledge or information to admit or deny the allegations set forth therein and therefore denies each and every allegation contained in paragraph 1.

2. In response to paragraph 2 of the First Amended Complaint, defendant Fairchild Semiconductor International, Inc. admits that it is a corporation duly incorporated under the laws of the State of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. Defendant Fairchild Semiconductor Corporation admits that it is a corporation

duly incorporated under the laws of the State of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. FAIRCHILD denies any and all remaining allegation of paragraph 2.

JURISDICTION AND VENUE

3. In response to paragraph 3 of the First Amended Complaint, FAIRCHILD denies that it has infringed or now infringes the patents asserted against FAIRCHILD in the First Amended Complaint. FAIRCHILD admits that the First Amended Complaint purports to state a cause of action under the patent laws of the United States, Title 35 U.S.C. § 1 *et seq.* FAIRCHILD admits that the First Amended Complaint purport to state a cause of action over which this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

4. In response to paragraph 4 of the First Amended Complaint, FAIRCHILD admits that this Court has personal jurisdiction over FAIRCHILD.

5. In response to paragraph 5 of the First Amended Complaint, FAIRCHILD admits, for the purpose of this action only, that venue is proper in this judicial district.

GENERAL ALLEGATIONS

6. In response to paragraph 6 of the First Amended Complaint, FAIRCHILD lacks sufficient knowledge or information to admit or deny the allegations set forth therein and therefore denies each and every allegation contained in paragraph 6.

7. In response to paragraph 7 of the First Amended Complaint, FAIRCHILD denies that it manufactures PWM integrated circuits devices in the United States. FAIRCHILD denies that it has been or currently is infringing, inducing infringement, or contributing to the infringement of the any PI patent asserted in the First Amended Complaint. FAIRCHILD admits that it imports a de minimis amount of PWM integrated circuits devices into the United States and that it sells and offers to sell a de minimis amount of PWM integrated circuits devices in the United States. FAIRCHILD denies any and all remaining allegations of paragraph 7 of the First Amended Complaint.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,107,851

8. In response to paragraph 8 of the First Amended Complaint, FAIRCHILD realleges its answers as set forth in paragraphs 1-7 above and incorporates by reference paragraphs 1 through 7, inclusive, as through fully set forth in this paragraph.

9. In response to paragraph 9 of the First Amended Complaint, FAIRCHILD admits that the title page of United States Patent No. 6,107,851 ("the '851 patent") states on its face that the patent was issued on August 22, 2000. FAIRCHILD admits that on its face the '851 patent is entitled "Offline Converter with Integrated Softstart and Frequency Jitter." FAIRCHILD admits that on its face the '851 patent lists "Power Integrations, Inc." as the assignee. FAIRCHILD admits that a copy of the '851 patent was attached to PI's original Complaint as Exhibit A. FAIRCHILD denies that the '851 patent is dully and legally issued. FAIRCHILD denies any and all remaining allegations of paragraph 9 of the First Amended Complaint.

10. In response to paragraph 10 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

11. In response to paragraph 11 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

12. In response to paragraph 12 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

13. In response to paragraph 13 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

SECOND CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,249,876

14. In response to paragraph 14 of the First Amended Complaint, FAIRCHILD realleges its answers as set forth in paragraphs 1-7 above and incorporates by reference paragraphs 1 through 7, inclusive, as through fully set forth in this paragraph.

15. In response to paragraph 15 of the First Amended Complaint, FAIRCHILD admits that the title page of United States Patent No. 6,249,876 ("the '876 patent") states on its face that the patent was issued on June 19, 2001. FAIRCHILD admits that on its face the '876 patent is entitled "Frequency Jittering Control for Varying the Switching Frequency of a Power Supply." FAIRCHILD admits that on its face the '876 patent lists "Power Integrations, Inc." as the assignee. FAIRCHILD admits that a copy of the '876 patent was attached to PI's original Complaint as Exhibit B. FAIRCHILD denies that the '876 patent is dully and legally issued. FAIRCHILD denies any and all remaining allegations of paragraph 15 of the First Amended Complaint.

16. In response to paragraph 16 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

17. In response to paragraph 17 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

18. In response to paragraph 18 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

19. In response to paragraph 19 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

THIRD CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,229,366

20. In response to paragraph 20 of the First Amended Complaint, FAIRCHILD realleges its answers as set forth in paragraphs 1-7 above and incorporates by reference paragraphs 1 through 7, inclusive, as through fully set forth in this paragraph.

21. In response to paragraph 21 of the First Amended Complaint, FAIRCHILD admits that the title page of United States Patent No. 6,229,366 ("the '366 patent") states on its face that the patent was issued on May 8, 2001. FAIRCHILD admits that on its face the '366 patent is entitled "Off-Line Converter with Integrated Softstart and Frequency Jitter." FAIRCHILD admits that on its face the '366 patent lists "Power Integrations, Inc." as the

assignee. FAIRCHILD admits that a copy of the '366 patent was attached to PI's original Complaint as Exhibit C. FAIRCHILD denies that the '366 patent is dully and legally issued. FAIRCHILD denies any and all remaining allegations of paragraph 21 of the First Amended Complaint.

22. In response to paragraph 22 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

23. In response to paragraph 23 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

24. In response to paragraph 24 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

25. In response to paragraph 25 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

FOURTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 4,811,075

26. In response to paragraph 26 of the First Amended Complaint, FAIRCHILD realleges its answers as set forth in paragraphs 1-7 above and incorporates by reference paragraphs 1 through 7, inclusive, as through fully set forth in this paragraph.

27. In response to paragraph 27 of the First Amended Complaint, FAIRCHILD admits that the title page of United States Patent No. 4,811,075 ("the '075 patent") states on its face that the patent was issued on March 7, 1989. FAIRCHILD admits that on its face the '075 patent is entitled "High Voltage MOS Transistors." FAIRCHILD admits that on its face the '075 patent lists "Power Integrations, Inc." as the assignee. FAIRCHILD admits that a copy of the '075 patent was attached to PI's original Complaint as Exhibit D. FAIRCHILD denies that the '075 patent is dully and legally issued. FAIRCHILD denies any and all remaining allegations of paragraph 27 of the First Amended Complaint.

28. In response to paragraph 28 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

29. In response to paragraph 29 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

30. In response to paragraph 30 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

31. In response to paragraph 31 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

AFFIRMATIVE AND OTHER DEFENSES

Further Answering the First Amended Complaint, FAIRCHILD asserts the following defenses. FAIRCHILD reserves the right to amend its answer with additional defenses as further information is obtained.

First Defense: Noninfringement of the Asserted Patents

32. FAIRCHILD has not infringed, contributed to infringement of, or induced the infringement of any valid claim of the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent, and is not liable for infringement thereof.

33. No product made by FAIRCHILD or process used by FAIRCHILD infringes the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent because PI's First Amended Complaint fails to state a claim that meets the requirements of 35 U.S.C. § 271.

Second Defense: Invalidity of the Asserted Patents

34. The '851 Patent, the '876 Patent, the '366 Patent, and the '075 Patent are invalid for failing to comply with the provisions of the Patent Laws, Title 35 U.S.C, including without limitation 35 U.S.C §§ 102, 103, 112, and 121.

Third Defense: Unavailability of Relief

35. PI has failed to plead and meet the requirements of 35 U.S.C. § 271(b) and (c) and is not entitled to any alleged damages from FAIRCHILD.

Fourth Defense: Unavailability of Relief (Marking and Notice)

36. PI has failed to plead and meet the requirements of 35 U.S.C. § 287 on marking and notice, and has otherwise failed to show that it is entitled to any damages prior to the filing date of the First Amended Complaint.

Fifth Defense: Limitation on Damages (Past Damages)

37. PI's claim for relief and prayer for damages are limited by 35 U.S.C. § 286.

Sixth Defense: Limitation on Damages (Increased Damages and Attorney Fees)

38. PI has failed to plead and meet the requirements of 35 U.S.C. § 284 and 285 for increased damages and attorney fees and is not entitled to any such increased damages or attorney fees.

Seventh Defense: Estoppel

39. PI is estopped from alleging that the '851 Patent, the '876 Patent, the '366 Patent, and/or the '075 Patent cover or include any accused product or activity by FAIRCHILD based on arguments made by PI during prosecution of the '851 Patent, the '876 Patent, the '366 Patent, and/or the '075 Patent.

Eighth Defense: Laches

40. On information and belief, PI's claims for relief are barred, in whole or in part, by the equitable doctrine of laches.

Ninth Defense: Waiver

41. On information and belief, PI's claims for relief are barred or unenforceable, in whole or in part, due to waiver.

Tenth Defense: Unenforceability

42. On information and belief, PI's claims for relief are unenforceable, in whole or in part, due to unclean hands.

Eleventh Defense: Unenforceability

43. On information and belief, PI's claims for relief are unenforceable, in whole or in part, due to inequitable conduct. FAIRCHILD incorporates by reference Paragraphs 24-89 of its COUNTERCLAIMS, as if fully restated herein.

COUNTERCLAIMS

First Counterclaim: Declaratory Judgment of Non-Infringement

1. This action arises under the patent laws of the United States, Title 35 U.S.C. §§ 1, *et seq*. This Court has subject matter jurisdiction over this counterclaim under 28 U.S.C. §§ 1331, 1338(a), 2201, and 2202.

2. Fairchild Semiconductor International, Inc. is a Delaware corporation with its principal place of business in South Portland, Maine. Fairchild Semiconductor Corporation is a Delaware corporation with its principal place of business in South Portland, Maine. (Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation are collectively referred to as "FAIRCHILD.")

3. On information and belief, Plaintiff/Counterclaim Defendant Power Integrations, Inc. ("PI") is a Delaware corporation with its principal place of business in San Jose, California.

4. Venue is proper in the District of Delaware pursuant to 28 U.S.C. §§ 1391(b)-(c) and 1400.

5. PI purports to be the owner of U.S. Patent Nos. 6,107,851 ("the '851 Patent"), 6,249,876 ("the '876 Patent"), 6,229,366 ("the '366 Patent"), and 4,811,075 ("the '075 Patent").

6. PI alleges that FAIRCHILD has infringed the '851 Patent, the '876 Patent, the '366 Patent, and the '075 Patent.

7. No product made by FAIRCHILD or process used by FAIRCHILD has infringed, either directly or indirectly, any claim of the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent, and FAIRCHILD is not liable for infringement thereof.

8. No activity by FAIRCHILD comes within the requirements of 35 U.S.C. § 271 with respect to the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent, and

FAIRCHILD is not liable for infringement of the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent under 35 U.S.C. § 271.

9. FAIRCHILD's activities that are outside of the United States do not come within the requirements of 35 U.S.C. § 271 with respect to the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent, and do not constitute infringement.

10. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to the infringement or noninfringement of the '851 Patent, the '876 Patent, the '366 Patent, and/or the '075 Patent.

Second Counterclaim: Declaratory Judgment of Invalidity of the '851 Patent

11. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

12. The '851 Patent, and each claim thereof, is invalid for failing to comply with the provisions of the Patent Laws, including one or more of 35 U.S.C. §§ 102, 103, 112, and 121.

13. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '851 Patent are valid or invalid.

Third Counterclaim: Declaratory Judgment of Invalidity of the '876 Patent

14. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

15. The '876 Patent, and each claim thereof, is invalid for failing to comply with the provisions of the Patent Laws, including one or more of 35 U.S.C. §§ 102, 103, 112, and 121.

16. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '876 Patent are valid or invalid.

Fourth Counterclaim: Declaratory Judgment of Invalidity of the '366 Patent

17. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

18. The '366 Patent, and each claim thereof, is invalid for failing to comply with the provisions of the Patent Laws, including one or more of 35 U.S.C. §§ 102, 103, 112, and 121.

19. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '366 Patent are valid or invalid.

Fifth Counterclaim: Declaratory Judgment of Invalidity of the '075 Patent

20. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

21. The '075 Patent, and each claim thereof, is invalid for failing to comply with the provisions of the Patent Laws, including one or more of 35 U.S.C. §§ 102, 103, 112, and 121.

22. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '075 Patent are valid or invalid.

Sixth Counterclaim: Declaratory Judgment of Unenforceability the '366 Patent

23. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

24. The '366 Patent, and each claim thereof, is unenforceable due to inequitable conduct during the prosecution of the '366 Patent.

25. During prosecution of the '366 Patent, Power Integrations failed to disclose to the United States Patent and Trademark Office ("PTO") prior art that was highly material to the patentability of the claims of the '366 patent under prosecution, and that Power Integrations knew or should have known would have been important to a reasonable examiner. The undisclosed prior art references include at least devices that anticipate or render obvious claims

of the '366 Patent, that were designed, manufactured, offered for sale and sold by Power Integrations more than a year before the application leading to the '366 Patent was filed.

26. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '366 Patent are enforceable or unenforceable.

Power Integrations' TOP100-4 TopSwitch Datasheets and Family of Devices

27. Power Integrations' TOP100-4 TopSwitch family of devices was and is highly material prior art to the patentability of the claims of the '366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipates claims of the '366 Patent. These devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. Power Integrations published in the United States datasheets describing its TOP100-4 TopSwitch family of devices at least as early as July 1996. A copy of such a datasheet is attached hereto as Exhibit A. This is more than a year before Power Integrations filed the application leading to the '366 Patent and thus the TOP100-4 TopSwitch family of devices and the Power Integrations datasheets describing those products are prior art to the '366 Patent.

28. The TOP100-4 TopSwitch family of devices and the datasheets describing those devices were and are highly material to the patentability of the '366 Patent because they teach every element of claims of the '366 Patent. The materiality of this prior art is demonstrated by the fact that Figure 1 from the Power Integrations TOP100-4 TopSwitch datasheet (described in that datasheet as a "typical application") is identical to Figure 2 of the '366 Patent, which the Applicants describe as their "invention" (except that the reference to the prior art TOP100-4 device is replaced with a black box PWM controller). *See*, '366 Patent, col. 4, lines 50-52 ("Fig. 2 is a presently preferred power supply utilizing an [sic] pulse width modulated switch according to the present invention."; *see also*, '366 Patent, col. 5, lines 3-column 6, line 34 (describing

Figure 2, identical to Figure 1 from the prior art TOP100-4 datasheet, as the "preferred embodiment".).

29. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed to the Patent Office either Power Integrations' TOP100-4 TopSwitch family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '366 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' TOP100-4 TopSwitch family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

Power Integrations' TOP200-4/14 TopSwitch Datasheets and Family of Devices

30. Power Integrations sold additional devices that anticipate the claims of the '366 Patent more than a year before the application leading to that patent was filed. For instance, Power Integrations published the TOP200-4/14 datasheet at least as early as November, 1994, a copy of which is attached hereto as Exhibit B. On information and belief, Power Integrations offered for sale and sold its TOP200-4/14 family of devices more than a year before the application leading to the '366 patent was filed.

31. As with the TOP100-4, the TOP200-4/14 (and datasheets describing these devices) were and are highly material to the patentability of the claims of the '366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipate claims of that patent. The materiality of this prior art is demonstrated by the fact that Figure 1 from the Power Integrations TOP200-4/14 TopSwitch datasheet (described in that datasheet as a "typical application") is identical to Figure 2 of the '366 Patent, which the

Applicants describe as their "invention" (except that the reference to the prior art TOP100-4 device is replaced with a black box PWM controller). *See*, '366 Patent, col. 4, lines 50-52 ("Fig. 2 is a presently preferred power supply utilizing an [sic] pulse width modulated switch according to the present invention."; *see also*, '366 Patent, col. 5, lines 3-column 6, line 34 (describing Figure 2, identical to figure 1 of the prior art TOP100-4 datasheet, as the "preferred embodiment".).

32. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed to the Patent Office either Power Integrations' TOP200-4/14 TopSwitch family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '366 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' TOP200-4/14 TopSwitch family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

Power Integrations' TOP221-227 TopSwitch Datasheets and Family of Devices

33. On information and belief, Power Integrations also offered for sale and sold the TOP221-227 TopSwitch-II family of devices prior to the filing of the application that led to the '366 Patent. Further, Power Integrations published in the United States datasheets describing the TOP221-227 TopSwitch-II family of devices at least as early as December, 1997, a copy of which is attached hereto as Exhibit C.

34. As described in the December 1997 datasheet, the prior art TOP221-227 TopSwitch-II family of devices anticipates claims of the '366 Patent. Thus, the TOP221-227 TopSwitch-II family of devices – and datasheets describing those devices – were and are highly material to the patentability of the '366 Patent, would have been important to a reasonable

examiner and would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the '366 Patent.

35. As with the TOP100-4 and TOP200-4/14 datasheets, Figure 1 from the TOP221-227 datasheet (described as a "typical flyback application") is identical to Figure 2 of the '366 Patent, which the Applicants describe as their "invention" (except that the reference to the prior art TOP100-4 device is replaced with a black box PWM controller). *See*, '366 Patent, col. 4, lines 50-52 ("Fig. 2 is a presently preferred power supply utilizing an [sic] pulse width modulated switch according to the present invention."; *see also*, '366 Patent, col. 5, lines 3-column 6, line 34 (describing Figure 2, identical to Figure 1 of the prior art TOP100-4 datasheet, as the "preferred embodiment".).

36. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed to the Patent Office either Power Integrations' TOP221-227 TopSwitch-II family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '366 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' TOP221-227 TopSwitch-II family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

Power Integrations' SMP260 Family of Devices and "Off-line Power Integrated Circuit for International Rated 60-watt Power Supplies" article.

37. Power Integrations also offered for sale and sold the PWR-SMP260 family of devices prior to the filing of the application that led to the '366 Patent. On information and belief, these products were also described in datasheets published by Power Integrations in the United States more than a year before Power Integrations filed the application leading to the '366 Patent. A copy of the SMP260 datasheet is attached as Exhibit D.

38. Power Integrations' PWR-SMP260 devices were also described in an article by Richard A. Keller entitled "Off-line Power Integrated Circuit for International Rated 60-watt Power Supplies", published in 1992, ("Keller Article"), a copy of which is attached as Exhibit F. Upon information and belief, at the time of the article Richard A. Keller was employed by Power Integrations.

39. Both the PWR-SMP260 devices and the Keller article were and are highly material prior art to the patentability of the claims of the '366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipate claims of the '366 Patent.

40. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed either the PWR-SMP260 devices or the Keller Article to the Patent Office during the prosecution of the '366 Patent.

41. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' PWR-SMP260 devices and the Keller Article, knew or should have known of the materiality of those devices and the Keller Article to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

Power Integrations' SMP240 Family of Devices

42. Power Integrations also offered for sale and sold the PWR-SMP240 family of devices prior to the filing of the application that led to the '366 Patent. On information and belief, these products were also described in datasheets published by Power Integrations in the United States more than a year before Power Integrations filed the application leading to the '366 Patent. A copy of the SMP240 datasheet is attached as Exhibit E.

43. The PWR-SMP240 devices was and is highly material prior art to the patentability of the claims of the '366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipate claims of the '366 Patent.

44. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed the PWR-SMP240 devices to the Patent Office during the prosecution of the '366 Patent.

45. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' PWR-SMP240 devices, knew or should have known of the materiality of those devices to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

Power Integrations' SMP211 Datasheets and Family of Devices

46. Power Integrations' SMP211 family of devices was and is highly material prior art to the patentability of the claims of the '366 Patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipates claims of the '366 Patent. These devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. Power Integrations published in the United States datasheets describing its SMP211 family of devices at least as early as 1996. A copy of such a datasheet is attached hereto as Exhibit G. This is more than a year before Power Integrations filed the application leading to the '366 Patent and thus the SMP211 family of devices and the Power Integrations datasheets describing those products are prior art to the '366 Patent.

47. The SMP211 family of devices and the datasheets describing those devices were and are highly material to the patentability of the '366 Patent because they teach every element

of claims of the '366 Patent. Figure 1 of the '366 Patent was described by the Applicants as the "Prior Art". This prior art figure includes a devices labeled "SMP211", which was a prior art Power Integrations device. The Applicants, however, withheld all information about their own SMP211 device from the Patent Examiner.

48. On December 13, 1999, during the prosecution of Application No. 09/080,774, the application that ultimately led to the issuance of the '366 Patent, the Examiner rejected pending claims as anticipated by Prior Art Figure 1:

> Claims 29, 35 & 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicants' Prior Art Fig. 1.
>
> Applicants' Prior Art Fig. 1 shows a first terminal 95, a second terminal Com, a switch/drive circuit 90 and a frequency variation circuit 140 as recited in claim 29.
>
> Further shown is a rectifier 10, a capacitor 15, a first winding 35 and a second winding 45 as recited in claim 35.
>
> Further shown is a feedback terminal (Error Amplifier in) as recited in claim 37.

The Examiner, however, allowed other claims because of his belief that the prior art did not include an oscillator that generated a maximum duty cycle signal and a signal with a frequency range depending on the frequency variation circuit:

> ***Allowable Subject Matter***
>
> The prior Art of record does not appear to disclose or suggest a PWM switch comprising an oscillator for generating a maximum duty cycle signal and a singnal [sic] with a frequency range dependant on a frequency variation circuit as recited in claim 1.

49. However, unknown to the Examiner, the SMP211 device referred to in Figure 1 of the '366 Patent actually included "an oscillator for generating a maximum duty cycle signal and a singnal [sic] with a frequency range dependant on a frequency variation circuit". *See* Exh. G, Figure 3 and 2-48 – 2-49. Thus, the SMP211 is highly relevant and material to the patentability of the '366 Patent. The Applicants, however, continued to withhold information concerning the SMP211 from the Examiner.

50. Rather than disclose the SMP211, the Applicants amended the rejected claims to include the oscillator limitation that the Examiner erroneously believed to be missing from the prior art of record:

> In the December 13, 1999 Office Action, claims 29, 35 and 37 are rejected under 35 U.S.C. § 102(b) as being anticipated by Applicants' Prior Art Figure 1.
>
> Claim 29 as presently amended now expressly recites a regulation circuit that includes an oscillator that provides a maximum duty cycle signal and an oscillation signal having a frequency range that is varied according to a frequency variation signal. The Applicants' Prior Art Figure 1 fails to disclose, teach or suggest such limitations. Accordingly, the Applicants respectfully submit that the instant section 102 rejection has been overcome.

51. Applicants' prior art SMP211 device – and datasheets describing the SMP211 device – clearly disclose "a regulation circuit that includes an oscillator that provides a maximum duty cycle signal and an oscillation signal having a frequency range that is varied according to a frequency variation signal." *See* Exh. G at Figure 3 and 2-48 – 2-49. Despite this, Applicants continued to withhold any information about their SMP211 devices. While withholding this information, the Applicants argued that the Examiner should allow the amended claims because Applicants had added limitations concerning the maximum duty cycle signal limitation, which they claimed was not present in the prior art of record (even though these limitations are present in the SMP211 devices and datasheets). Thereafter, the Examiner allowed the amended claims based upon the Applicants' false representations regarding the absence of a maximum duty cycle signal from the prior art.

52. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed to the Patent Office either Power Integrations' SMP211 family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '366 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP211 family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this

highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

Power Integrations' SMP3 Family of Devices, Datasheets, and "Off-Line PWM Switching Regulator IC Handles 3W" Article

53. In addition, Power Integrations' SMP3 family of devices was and is highly material prior art to the patentability of the claims of the '366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipates claims of the '366 Patent. On information and belief, these devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. These devices are described in an article entitled "Off-Line PWM Switching Regulator IC Handles 3W" by F. Goodenough, published on March 22, 1990 in *Electronic Design* (pp. 35-39) ("Goodenough Article"). A copy of the Goodenough Article is attached hereto as Exhibit I.

54. On information and belief, F. Goodenough was employed by Power Integrations when he wrote and published the Goodenough Article.

55. The prior art SMP3 devices and the Goodenough Article were and are highly material to the patentability of the '851 Patent as both the devices and the Article anticipate claims of that Patent.

56. Despite the highly material nature of the Power Integrations SMP3 devices and the Goodenough Article, neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed either the Power Integrations SMP3 devices or the Goodenough Article to the Patent Office during the prosecution of the '851 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP3 family of devices and the Goodenough Article describing those devices, knew or should have known of the materiality of those devices and Article to the patentability of the pending claims that issued in the '851 Patent,

and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Seventh Counterclaim: Declaratory Judgment of Unenforceability the '851 Patent

57. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

58. The '851 Patent, and each claim thereof, is unenforceable due to the inequitable conduct during the prosecution of the '851 Patent.

59. During the prosecution of the '851 Patent, Power Integrations failed to disclose to the United States Patent and Trademark Office prior art that was highly material to the patentability of the claims of the '851 Patent, and that Power Integrations knew or should have known would have been important to a reasonable examiner. The undisclosed prior art references include at least devices that anticipate or render obvious claims of the '851 Patent, that were designed, manufactured, offered for sale and sold by Power Integrations more than a year before the application leading to the '851 Patent was filed.

60. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '851 Patent are enforceable or unenforceable.

Power Integrations' SMP402 Datasheets and Family of Devices

61. Power Integrations' SMP402 family of devices was and is highly material prior art to the patentability of the claims of the '851 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '851 Patent and anticipates claims of the '851 Patent. On information and belief, these devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. Power Integrations published datasheets in the United States describing its SMP402 family of devices at least as early as January, 1996. A copy of such a datasheet is attached hereto as Exhibit H. This is more than a year before Power Integrations filed the application leading to the '851 Patent and thus the

SMP402 family of devices and the Power Integrations datasheets describing those products are prior art to the '851 Patent.

62. The SMP402 family of devices and the datasheets describing those devices were and are highly material to the patentability of the '851 Patent because they teach every element of claims of the '851 Patent.

63. Power Integrations failed to disclose to the Patent Office either Power Integrations' SMP402 family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '851 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP402 family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '851 Patent, and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Power Integrations' SMP3 Family of Devices, Datasheets, and "Off-Line PWM Switching Regulator IC Handles 3W" Article

64. In addition, Power Integrations' SMP3 family of devices was and is highly material prior art to the patentability of the claims of the '851 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '851 Patent and anticipates claims of the '851 Patent. On information and belief, these devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. These devices are described in an article entitled "Off-Line PWM Switching Regulator IC Handles 3W" by F. Goodenough, published on March 22, 1990 in *Electronic Design* (pp. 35-39) ("Goodenough Article"). A copy of the Goodenough Article is attached hereto as Exhibit I.

65. On information and belief, F. Goodenough was employed by Power Integrations when he wrote and published the Goodenough Article.

66. The prior art SMP3 devices and the Goodenough Article were and are highly material to the patentability of the '851 Patent as both the devices and the Article anticipate claims of that Patent.

67. Despite the highly material nature of the Power Integrations SMP3 devices and the Goodenough Article, neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed either the Power Integrations SMP3 devices or the Goodenough Article to the Patent Office during the prosecution of the '851 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP3 family of devices and the Goodenough Article describing those devices, knew or should have known of the materiality of those devices and Article to the patentability of the pending claims that issued in the '851 Patent, and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Power Integrations' SMP260 Datasheets, Family of Devices, and "Off-line Power Integrated Circuit for International Rated 60-watt Power Supplies" Article

68. Power Integrations also offered for sale and sold the PWR-SMP260 family of devices prior to the filing of the application that led to the '851 Patent. On information and belief, these products were also described in datasheets published by Power Integrations in the United States more than a year before Power Integrations filed the application leading to the '851 Patent. A copy of the SMP260 datasheet is attached as Exhibit D.

69. Power Integrations' PWR-SMP260 devices were also described in an article by Richard A. Keller entitled "Off-line Power Integrated Circuit for International Rated 60-watt Power Supplies", published in 1992, ("Keller Article"), a copy of which is attached as Exhibit F. Upon information and belief, at the time of the article Richard A. Keller was employed by Power Integrations.

70. The PWR-SMP260 devices and the Keller article were and are both material to the patentability of the '851 Patent as both anticipate claims of that patent.

71. Neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed either the PWR-SMP260 devices or the Keller Article to the Patent Office during the prosecution of the '851 Patent.

72. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' PWR-SMP260 devices and the Keller Article, knew or should have known of the materiality of those devices and Article to the patentability of the pending claims that issued in the '851 Patent, and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Power Integrations' SMP240 Family of Devices

73. Power Integrations also offered for sale and sold the PWR-SMP240 family of devices prior to the filing of the application that led to the '851 Patent. On information and belief, these products were also described in datasheets published by Power Integrations in the United States more than a year before Power Integrations filed the application leading to the '851 Patent. A copy of the SMP240 datasheet is attached as Exhibit E.

74. The PWR-SMP240 devices was and is highly material prior art to the patentability of the claims of the '851 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '851 Patent and anticipate claims of the '851 Patent.

75. Neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed the PWR-SMP240 devices to the Patent Office during the prosecution of the '851 Patent.

76. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' PWR-SMP240 devices, knew or should have known of the materiality of those

devices to the patentability of the pending claims that issued in the '851 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Power Integrations' SMP211 Datasheets and Family of Devices

77. Power Integrations' SMP211 family of devices was and is highly material prior art to the patentability of the claims of the '851 Patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '851 Patent and anticipates claims of the '851 Patent. These devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. Power Integrations published in the United States datasheets describing its SMP211 family of devices at least as early as 1996. A copy of such a datasheet is attached hereto as Exhibit G. This is more than a year before Power Integrations filed the application leading to the '851 Patent and thus the SMP211 family of devices and the Power Integrations datasheets describing those products are prior art to the '851 Patent.

78. The SMP211 family of devices and the datasheets describing those devices were and are highly material to the patentability of the '851 Patent because they teach every element of claims of the '851 Patent. Figure 1 of the '851 Patent was described by the Applicants as the "Prior Art". This prior art figure includes a devices labeled "SMP211", which was a prior art Power Integrations device. The Applicants, however, withheld all information about their own SMP211 device from the Patent Examiner.

79. On December 13, 1999, during the prosecution of the '851 Patent, the Examiner rejected pending claims as anticipated by Prior Art Figure 1:

> Claims 29, 35 & 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicants' Prior Art Fig. 1.
>
> Applicants' Prior Art Fig. 1 shows a first terminal 95, a second terminal Com, a switch/drive circuit 90 and a frequency variation circuit 140 as recited in claim 29.
>
> Further shown is a rectifier 10, a capacitor 15, a first winding 35 and a second winding 45 as recited in claim 35.

Further shown is a feedback terminal (Error Amplifier in) as recited in claim 37. The Examiner, however, allowed other claims because of his belief that the prior art did not include an oscillator that generated a maximum duty cycle signal and a signal with a frequency range depending on the frequency variation circuit:

Allowable Subject Matter

> The prior Art of record does not appear to disclose or suggest a PWM switch comprising an oscillator for generating a maximum duty cycle signal and a singnal [sic] with a frequency range dependant on a frequency variation circuit as recited in claim 1.

80. However, unknown to the Examiner, the SMP211 device referred to in Figure 1 of the '851 Patent actually included "an oscillator for generating a maximum duty cycle signal and a singnal [sic] with a frequency range dependant on a frequency variation circuit". *See* Exh. G, Figure 3 and 2-48 – 2-49. Thus, the SMP211 is highly relevant and material to the patentability of the '851 Patent. The Applicants, however, continued to withhold information concerning the SMP211 from the Examiner.

81. Rather than disclose the SMP211, the Applicants amended the rejected claims to include the oscillator limitation that the Examiner erroneously believed to be missing from the prior art of record:

> In the December 13, 1999 Office Action, claims 29, 35 and 37 are rejected under 35 U.S.C. § 102(b) as being anticipated by Applicants' Prior Art Figure 1.
>
> Claim 29 as presently amended now expressly recites a regulation circuit that includes an oscillator that provides a maximum duty cycle signal and an oscillation signal having a frequency range that is varied according to a frequency variation signal. The Applicants' Prior Art Figure 1 fails to disclose, teach or suggest such limitations. Accordingly, the Applicants respectfully submit that the instant section 102 rejection has been overcome.

82. Applicants' prior art SMP211 device – and datasheets describing the SMP211 device – clearly disclose "a regulation circuit that includes an oscillator that provides a maximum duty cycle signal and an oscillation signal having a frequency range that is varied according to a frequency variation signal." *See* Exh. G at Figure 3 and 2-48 – 2-49. Despite this, Applicants continued to withhold any information about their SMP211 devices. While withholding this information, the Applicants argued that the Examiner should allow the amended claims because

Applicants had added limitations concerning the maximum duty cycle signal limitation, which they claimed was not present in the prior art of record (even though these limitations are present in the SMP211 devices and datasheets). Thereafter, the Examiner allowed the amended claims based upon the Applicants' false representations regarding the absence of a maximum duty cycle signal from the prior art.

83. Neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed to the Patent Office either Power Integrations' SMP211 family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '851 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP211 family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '851 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Seventh Counterclaim: Declaratory Judgment of Unenforceability the '876 Patent

84. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

85. The '876 Patent, and each claim thereof, is unenforceable due to inequitable conduct during the prosecution of the '876 Patent.

86. During prosecution of the '876 Patent, Power Integrations failed to disclose to the United States Patent and Trademark Office ("PTO") prior art that was highly material to the patentability of the claims of the '876 patent under prosecution, and that Power Integrations knew or should have known would have been important to a reasonable examiner. The undisclosed prior art references include at least Power Integrations public disclosure of the technology described in Power Integrations '851 Patent.

87. Power Integrations purports to have invented the invention claimed in the '876 Patent on May 21, 1998. On information and belief, on September 2, 1997 and over eight months before the date of the alleged invention claimed in the '876 Patent, Power Integrations made public disclosure of the alleged invention of the '851 Patent. Thus, the alleged invention of the '851 Patent is prior art to the alleged invention of the '876 Patent pursuant to 35 U.S.C. § 102(a).

88. Indeed, in their Invention Disclosure Form, the inventors of the '876 Patent describe the alleged invention of the '851 Patent as "PRIOR ART" and include a Figure labeled "Frequency Jittering Prior Art." Power Integrations, however, never informed the Patent Office that the '851 Patent was prior art to the '876 Patent. Power Integrations included the figure from its Invention Disclosure Form that it had previously identified as "PRIOR ART" as Figure 3 of the '876 Patent. Rather than inform the Patent Office that this Figure depicted the prior art, Power Integrations simply stated that "FIG. 3 is a schematic diagram of an analog frequency jittering device" and incorporated the '851 Patent by reference into the specification of the '876 Patent.

89. The '851 Patent and the public disclosure of devices that embody the '851 Patent are highly material to the patentability of the claims of the '876 Patent and Power Integrations knew or should have known that they would have been important to a reasonable examiner.

90. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '876 Patent are enforceable or unenforceable.

Eighth Counterclaim: Declaratory Judgment of Unenforceability the '075 Patent

91. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

92. The '075 Patent, and each claim thereof, is unenforceable due to inequitable conduct during the prosecution of the '075 Patent.

93. During prosecution of the '075 Patent, the Applicant, Klaus Eklund, and his attorneys failed to disclose to the United States Patent and Trademark Office ("PTO") prior art that was highly material to the patentability of the claims of the '075 patent under prosecution, and that Mr. Eklund and his attorneys knew or should have known would have been important to a reasonable examiner. The undisclosed prior art references include at least technical articles known to Mr. Eklund that were published more than a year before the application leading to the '075 Patent was filed.

94. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '075 Patent are enforceable or unenforceable.

***A Highly Reliable 16 Output High Voltage NMOS/CMOS Logic IC with Shielded Source Structure*, by H. Wakaumi, T. Suzuki, M. Saito and H. Sakuma, IEDM 83, pp. 416-419 (1983) and *High-Voltage DMOS and PMOS in Analog IC's* by A.W. Ludikhuize, IEDM 82, pp. 81-84 (1982).**

95. The article "*A Highly Reliable 16 Output High Voltage NMOS/CMOS Logic IC with Shielded Source Structure*", by H. Wakaumi, T. Suzuki, M. Saito and H. Sakuma ("Wakaumi Article") and the article *"High-Voltage DMOS and PMOS in Analog IC's"* by A.W. Ludikhuize ("Ludikhuize Article") are highly material prior art to the patentability of the claims of the '075 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Mr. Eklund prosecuted in the application for the '075 Patent. The Wakaumi Article was published in the IEDM journal at least as early as 1983. A copy of the Wakaumi Article is attached hereto as Exhibit J. The Ludikhuize Article was published in the IEDM journal at least as early as 1982. A copy of the Ludikhuize Article is attached hereto as Exhibit K. Since both articles were published more than a year before Power Integrations filed the application leading to the '075 Patent, they are prior art to the '075 Patent.

96. The materiality of the Wakaumi and Ludikhuize Articles is demonstrated by the fact that Mr. Eklund was aware of both articles at the time he allegedly conceived of the '075 Patent, considered the articles to be "key" references, and specifically identified at least the

Wakaumi Article in notes that he now claims describe the invention leading to the '075 Patent. Indeed, one of ordinary skill in the art would have been motivated to combine the Wakaumi and Ludikhuize Articles and the combination of these Articles meets every element of each asserted claim of the '075 Patent. Thus, the claims of the '075 Patent are obvious in light of the Wakaumi and Ludikhuize Articles.

97. Despite his admitted knowledge and appreciation of the Wakaumi and Ludikhuize Articles, neither Mr. Eklund nor his attorneys disclosed either Article to the Patent Office during the prosecution of the '075 Patent. This constitutes inequitable conduct that renders all claims of the '075 Patent permanently unenforceable.

PRAYER FOR RELIEF

WHEREFORE, FAIRCHILD prays for the following relief:

A. The Court enter judgment against PI, and dismiss with prejudice, any and all claims of PI's First Amended Complaint for Patent Infringement; and order that Plaintiff take nothing as a result of the First Amended Complaint;

B. The Court enter judgment declaring that FAIRCHILD has not infringed, contributed to infringement of, or induced infringement of the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent;

C. The Court enter judgment declaring that the '851 Patent, the '876 Patent, the '366 Patent, and the '075 Patent are invalid;

D. The Court enter judgment declaring that the '851 Patent, the '876 Patent, the '366 Patent, and the '075 Patent are unenforceable;

E. The Court award to FAIRCHILD its reasonable costs and attorneys' fees against PI pursuant to the provisions of 35 U.S.C. § 285;

F. The Court award to FAIRCHILD pre-judgment interest and costs of this action; and,

G. The Court grant to FAIRCHILD such other and further relief as may be deemed just and appropriate.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure and Rule 38.1 of the Local Rules of the United States District Court for the District of Delaware, Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation hereby demand a trial by jury on this action.

ASHBY & GEDDES

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Dated: February 23, 2006
166925.1

EXHIBIT A

TOP100-4

TOPSwitch® Family

Three-terminal Off-line PWM Switch

POWER INTEGRATIONS, INC.

Product Highlights

Low Cost Replacement for Discrete Switchers
- 20 to 50 fewer components - cuts cost, increases reliability
- Source-connected tab and Controlled MOSFET turn-on reduce EMI and EMI filter costs
- Allows for a 50% smaller and lighter solution
- Cost competitive with linears above 5 W

Up to 90% Efficiency in Flyback Topology
- Built-in start-up and current limit reduce DC losses
- Low capacitance 350 V MOSFET cuts AC losses
- CMOS controller/gate driver consumes only 6 mW
- 70% maximum duty cycle minimizes conduction losses

Simplifies Design - Reduces Time to Market
- Supported by many reference designs
- Integrated PWM Controller and 350 V MOSFET in a industry standard three pin TO-220 package
- Only one external capacitor needed for compensation, bypass and start-up/auto-restart functions

System Level Fault Protection Features
- Auto-restart and cycle by cycle current limiting functions handle both primary and secondary faults
- On-chip latching thermal shutdown protects the entire system against overload

Highly Versatile
- Implements Buck, Boost, Flyback or Forward topology
- Easily interfaces with both opto and primary feedback
- Supports continuous or discontinuous mode of operation
- Specified for operation down to 16 V DC input

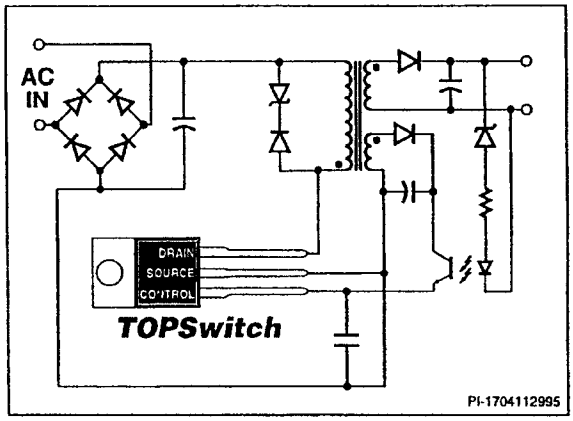


Figure 1. Typical Application.

TOPSwitch SELECTION GUIDE

ORDER PART NUMBER	OUTPUT POWER RANGE		
	FLYBACK		PFC/ BOOST
	100/110 V VAC	48 V DC	100/110 VAC
TOP100YAI*	0-20 W	0-6.8 W	0-30 W
TOP101YAI*	15-35 W	6-12 W	25-50 W
TOP102YAI*	20-45 W	8.5-17 W	35-70 W
TOP103YAI*	25-55 W	11-22 W	45-90 W
TOP104YAI*	30-60 W	12-25 W	55-110 W

* Package Outline: Y03A

Description

The *TOPSwitch* family implements, with only three pins, all functions necessary for an off-line switched mode control system: high voltage N-channel power MOSFET with controlled turn-on gate driver, voltage mode PWM controller with integrated 100 kHz oscillator, high voltage start-up bias circuit, bandgap derived reference, bias shunt regulator/error amplifier for loop compensation and fault protection circuitry. Compared to discrete MOSFET and controller or self oscillating (RCC) switching converter solutions, a *TOPSwitch* integrated circuit can reduce total cost, component count, size, weight and at the same time increase efficiency and system reliability. These devices are intended for 100/110 VAC off-line Power Supply applications in the 0 to 60 W range and power factor correction (PFC) applications in the 0 to 110 W range. They are also well suited for Telecom, Cablecom and other DC to DC converter applications in the 0-25 W range (see Design Note DN-16).

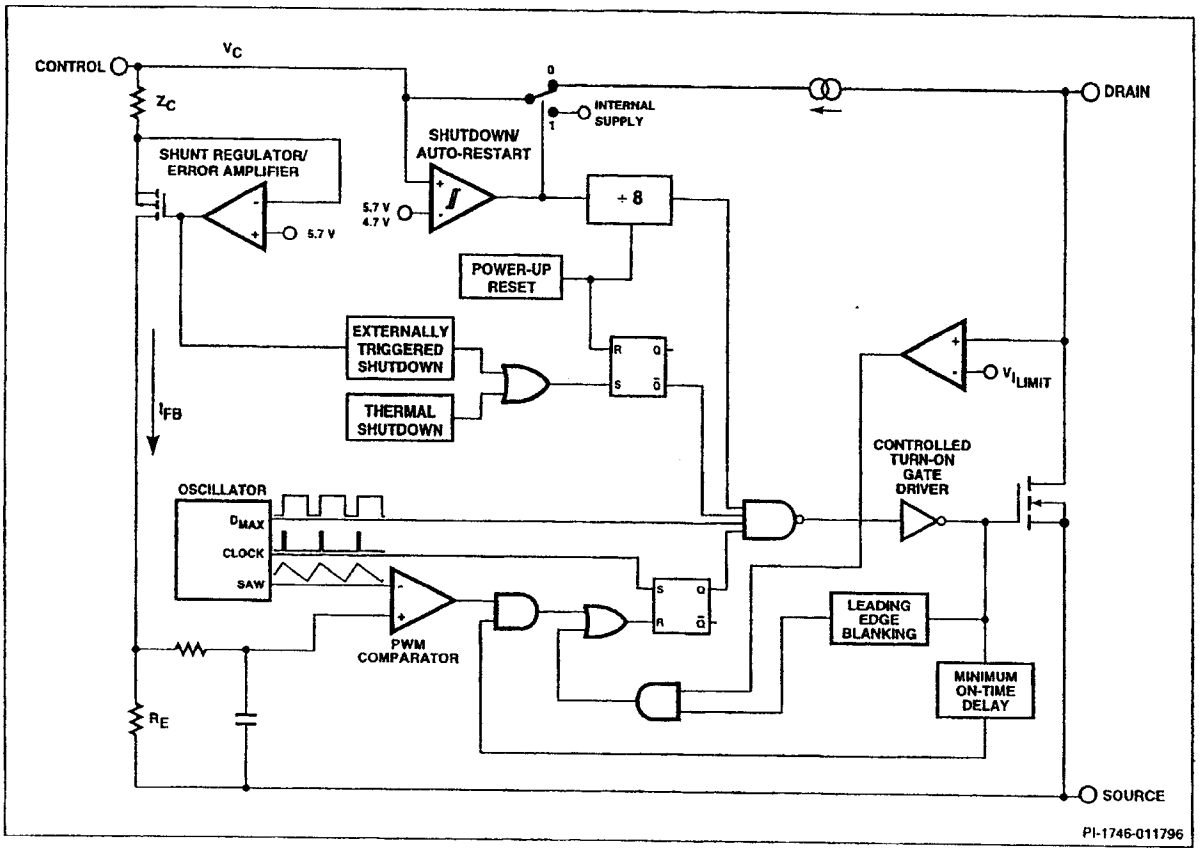


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN Pin:
Output MOSFET drain connection. Provides internal bias current during start-up operation via an internal switched high-voltage current source. Internal current sense point.

CONTROL Pin:
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. Trigger input for latching shutdown. It is also used as the supply bypass and auto-restart/ compensation capacitor connection point.

SOURCE Pin:
Output MOSFET source connection. Primary-side circuit common, power return, and reference point.

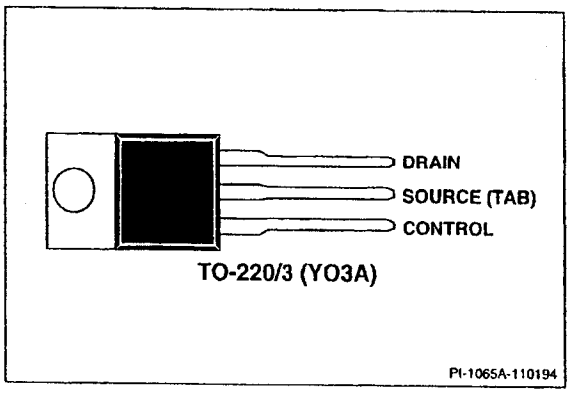


Figure 3. Pin Configuration.

TOPSwitch Family Functional Description

TOPSwitch is a self biased and protected linear control current-to-duty cycle converter with an open drain output. High efficiency is achieved through the use of CMOS and integration of the maximum number of functions possible. CMOS significantly reduces bias currents as compared to bipolar or discrete solutions. Integration eliminates external power resistors used for current sensing and/or supplying initial start-up bias current.

During normal operation, the internal output MOSFET duty cycle linearly decreases with increasing CONTROL pin current as shown in Figure 4. To implement all the required control, bias, and protection functions, the DRAIN and CONTROL pins each perform several functions as described below. Refer to Figure 2 for a block diagram and Figure 6 for timing and voltage waveforms of the *TOPSwitch* integrated circuit.

Control Voltage Supply

CONTROL pin voltage V_C is the supply or bias voltage for the controller and driver circuitry. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the gate drive current. The total amount of capacitance connected to this pin (C_T) also sets the auto-restart timing as well as control loop compensation. V_C is regulated in either of two modes of operation. Hysteretic regulation is used for initial start-up and overload operation. Shunt regulation is used to separate the duty cycle error signal from the control circuit supply current. During start-up, V_C current is supplied from a high-voltage switched current source connected internally between the DRAIN and CONTROL pins. The current source provides sufficient current to supply the control circuitry as well as charge the total external capacitance (C_T).

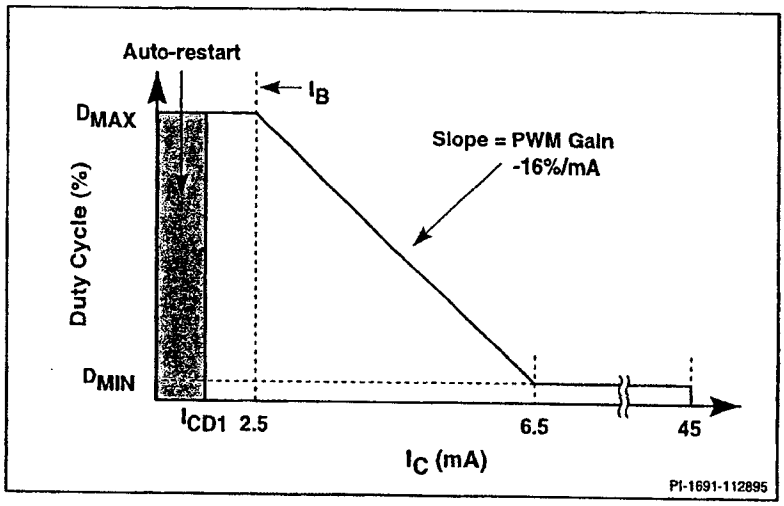


Figure 4. Relationship of Duty Cycle to CONTROL Pin Current.

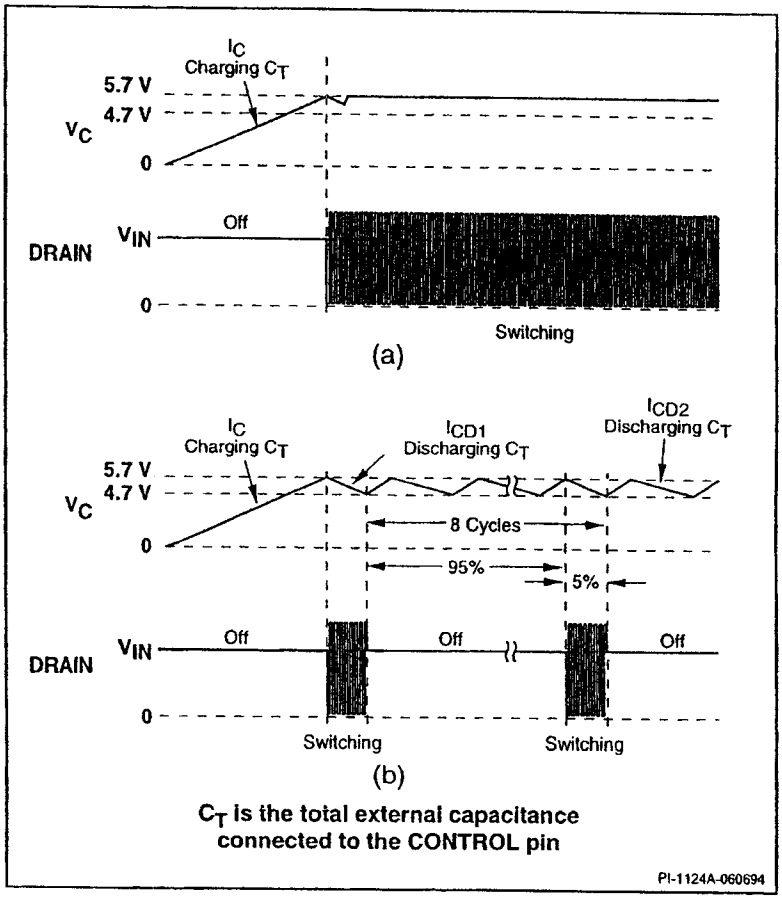


Figure 5. Start-up Waveforms for (a) Normal Operation and (b) Auto-restart.

TOPSwitch Family Functional Description (cont.)

The first time V_C reaches the upper threshold, the high-voltage current source is turned off and the PWM modulator and output transistor are activated, as shown in Figure 5(a). During normal operation (when the output voltage is regulated) feedback control current supplies the V_C supply current. The shunt regulator keeps V_C at typically 5.7 V by shunting CONTROL pin feedback current exceeding the required DC supply current through the PWM error signal sense resistor R_E. The low dynamic impedance of this pin (Z_C) sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance of the CONTROL pin together with the external resistance and capacitance determines the control loop compensation of the power system.

If the CONTROL pin external capacitance (C_T) should discharge to the lower threshold, then the output MOSFET is turned off and the control circuit is placed in a low-current standby mode. The high-voltage current source is turned on and charges the external capacitance again. Charging current is shown with a negative polarity and discharging current is shown with a positive polarity in Figure 6. The hysteretic auto-restart comparator keeps V_C within a window of typically 4.7 to 5.7 V by turning the high-voltage current source on and off as shown in Figure 5(b). The auto-restart circuit has a divide-by-8 counter which prevents the output MOSFET from turning on again until eight discharge-charge cycles have elapsed. The counter effectively limits *TOPSwitch* power dissipation by reducing the auto-restart duty cycle to typically 5%. Auto-restart continues to cycle until output voltage regulation is again achieved.

Bandgap Reference

All critical *TOPSwitch* internal voltages are derived from a temperature-compensated bandgap reference. This reference is also used to generate a temperature-compensated current source which is trimmed to accurately set the oscillator frequency and MOSFET gate drive current.

Oscillator

The internal oscillator linearly charges and discharges the internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle. The nominal frequency of 100 kHz was chosen to minimize EMI and maximize efficiency in power supply applications. Trimming of the current reference improves oscillator frequency accuracy.

Pulse Width Modulator

The pulse width modulator implements a voltage-mode control loop by driving the output MOSFET with a duty cycle inversely proportional to the current flowing into the CONTROL pin. The error signal across R_E is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise. The filtered error signal is compared with the internal oscillator sawtooth waveform to generate the duty cycle waveform. As the control current increases, the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the output MOSFET. The pulse width modulator resets the latch, turning off the output MOSFET. The maximum duty cycle is set by the symmetry of the internal oscillator. The modulator has a minimum ON-time to keep the current consumption of the *TOPSwitch* independent of the error signal. Note that a minimum current must be driven into the CONTROL pin before the duty cycle begins to change.

Gate Driver

The gate driver is designed to turn the output MOSFET on at a controlled rate to minimize common-mode EMI. The gate drive current is trimmed for improved accuracy.

Error Amplifier

The shunt regulator can also perform the function of an error amplifier in primary feedback applications. The shunt regulator voltage is accurately derived from the temperature compensated bandgap reference. The gain of the error amplifier is set by the CONTROL pin dynamic impedance. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and flows through R_E as the error signal.

Cycle-By-Cycle Current Limit

The cycle by cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET ON-state drain-source voltage, $V_{DS(ON)}$, with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize variation of the effective peak current limit due to temperature related changes in output MOSFET $R_{DS(ON)}$.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that current spikes caused by primary-side capacitances and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

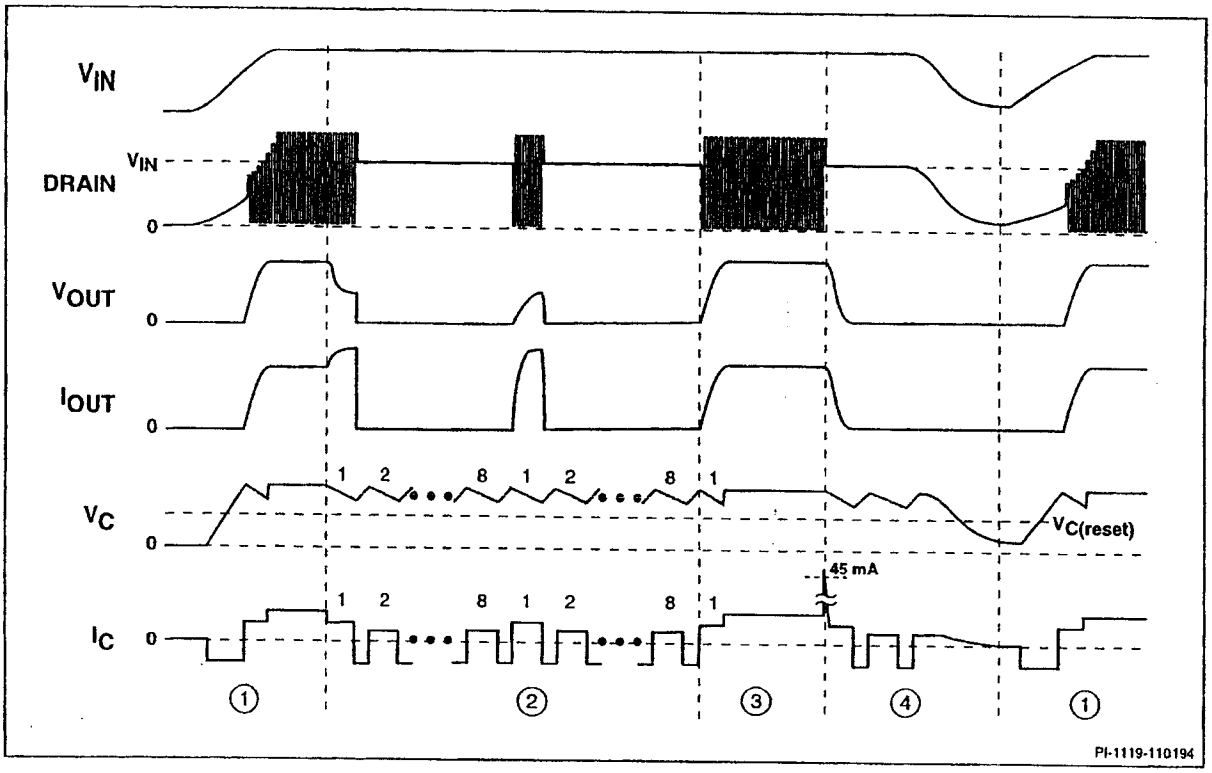


Figure 6. Typical Waveforms for (1) Normal Operation, (2) Auto-restart, (3) Latching Shutdown, and (4) Power Down Reset.

Shutdown/Auto-restart

To minimize *TOPSwitch* power dissipation, the shutdown/auto-restart circuit turns the power supply on and off at a duty cycle of typically 5% if an out of regulation condition persists. Loss of regulation interrupts the external current into the CONTROL pin. V_C regulation changes from shunt mode to the hysteretic auto-restart mode described above. When the fault condition is removed, the power supply output becomes regulated, V_C regulation returns to shunt mode, and normal operation of the power supply resumes.

Latching Shutdown

The output overvoltage protection latch is activated by a high-current pulse into the CONTROL pin. When set, the latch turns off the *TOPSwitch* output. Activating the power-up reset circuit by removing and restoring input power, or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. V_C is regulated in hysteretic mode when the power supply is latched off.

Overtemperature Protection

Temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (typically 145°C). Activating the power-up reset circuit by removing and restoring input power or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. V_C is regulated in hysteretic mode when the power supply is latched off.

High-voltage Bias Current Source

This current source biases *TOPSwitch* from the DRAIN pin and charges the CONTROL pin external capacitance (C_T) during start-up or hysteretic operation. Hysteretic operation occurs during auto-restart and latched shutdown. The current source is switched on and off with an effective duty cycle of approximately 35%. This duty cycle is determined by the ratio of CONTROL pin charge (I_C) and discharge currents (I_{CD1} and I_{CD2}). This current source is turned off during normal operation when the output MOSFET is switching.

General Circuit Operation

Primary Feedback Regulation

The circuit shown in Figure 7 is a simple 5 V, 5 W bias supply using the TOP100. This flyback power supply employs primary-side regulation from a transformer bias winding. This approach is best for low-cost applications requiring isolation and operation within a narrow range of load variation. Line and load regulation of ±5% or better can be achieved from 10% to 100% of rated load.

Voltage feedback is obtained from the transformer (T1) bias winding, which eliminates the need for optocoupler and secondary-referenced error amplifier. High-voltage DC is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated high-voltage MOSFET transistor within the TOP100 (U1). The circuit operates at a switching frequency of 100 kHz, set by the internal oscillator of the TOP100. The clamp circuit implemented by VR1 and D1 limits the leading-edge voltage spike caused by transformer leakage inductance to a safe value. The 5 V power secondary winding is rectified and filtered by D2, C2, C3, and L1 to create the 5 V output voltage.

The output of the T1 bias winding is rectified and filtered by D3, R1, and C5. The voltage across C5 is regulated by U1, and is determined by the 5.7 V internal shunt regulator at the CONTROL pin of U1. When the rectified bias voltage on C5 begins to exceed the shunt regulator voltage, current will flow into the control pin. Increasing control pin current decreases the duty cycle until a stable operating point is reached. The output voltage is proportional to the bias voltage by the turns ratio of the output to bias windings. C5 is used to bypass the CONTROL pin. C5 also provides loop compensation for the power supply by shunting AC currents around the CONTROL pin dynamic impedance, and also determines the auto-restart frequency during start-up and auto-restart conditions. See DN-8 for more information regarding bias supplies.

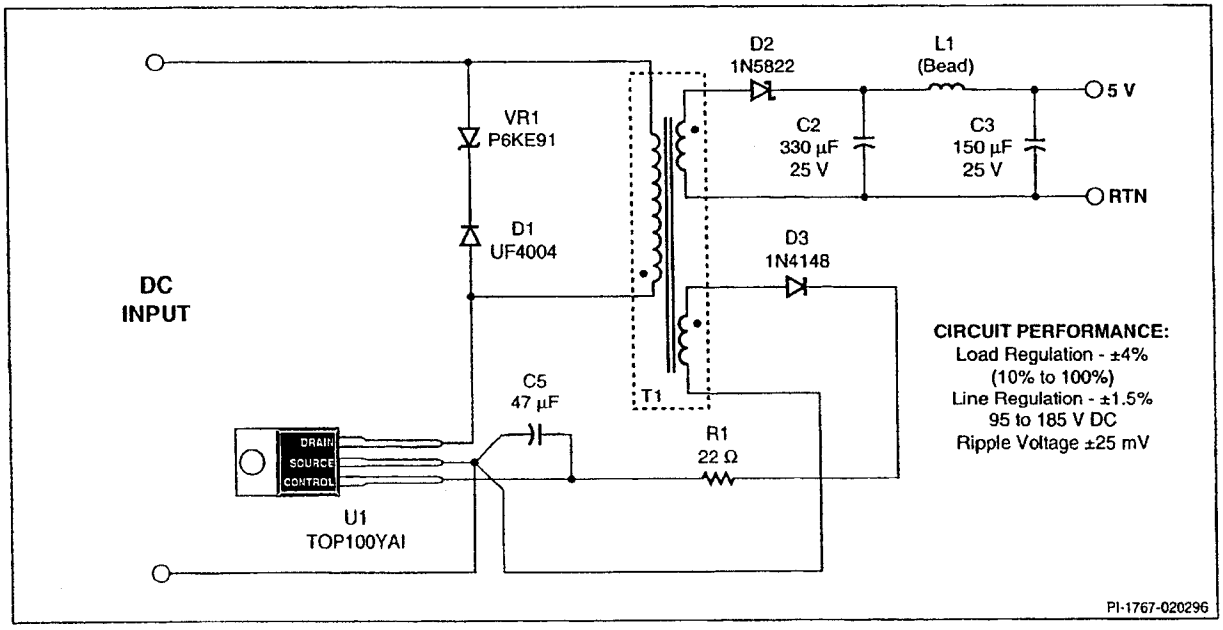


Figure 7. Schematic Diagram of a Minimum Parts Count 5 V, 5 W Bias Supply Utilizing the TOP100.

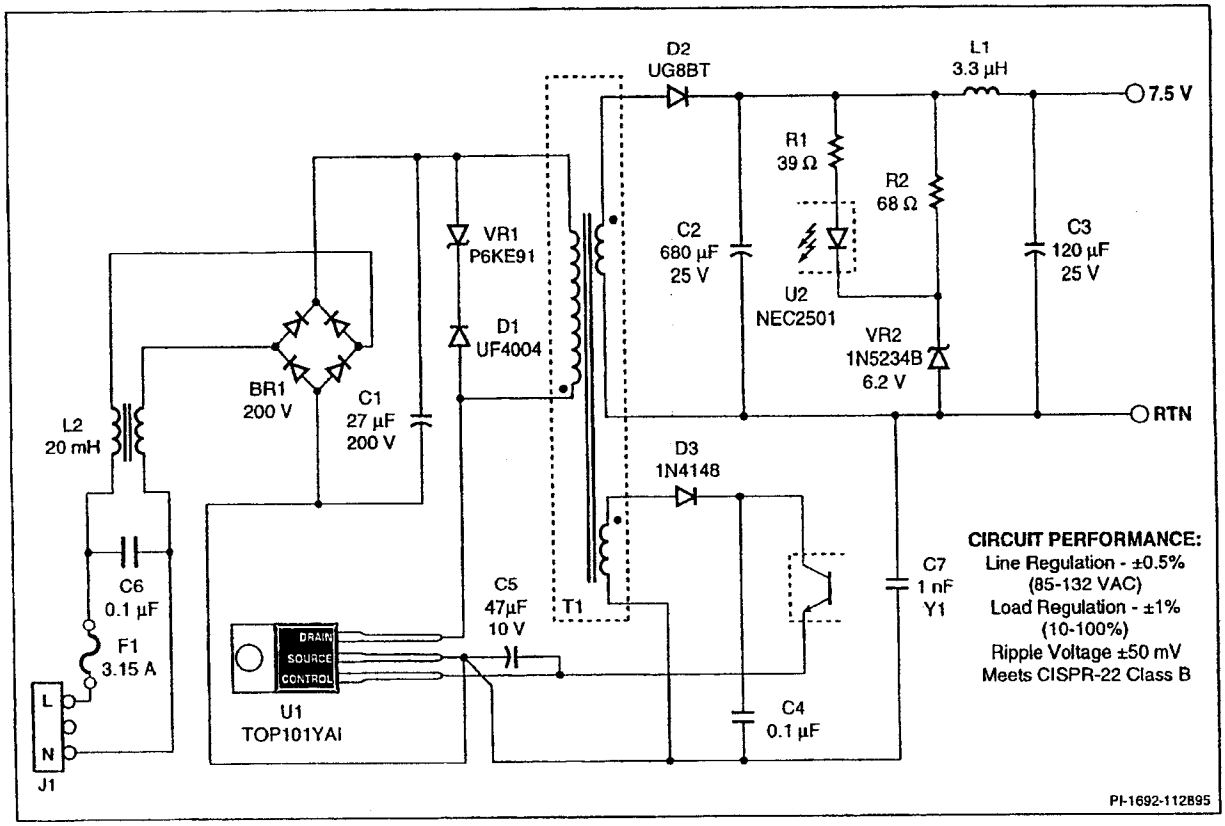


Figure 8. Schematic Diagram of a 15 W 100/110 VAC Input Power Supply Utilizing the TOP101 and Simple Optocoupler Feedback.

Simple Optocoupler Feedback

The circuit shown in Figure 8 is a 7.5 V, 15 W secondary regulated flyback power supply using the TOP101 that will operate from 85 to 132 VAC input voltage. Improved output voltage accuracy and regulation over the circuit of Figure 7 is achieved by using an optocoupler and secondary referenced Zener diode. The general operation of the power stage of this circuit is the same as that described for Figure 7.

The input voltage is rectified and filtered by BR1 and C1. L2, C6 and C7 reduce conducted emission currents. The bias winding is rectified and filtered by D3 and C4 to create a typical 11 V bias voltage. Zener diode (VR2) voltage together with the forward voltage of the LED in the optocoupler U2 determine the output voltage. R1, the optocoupler current transfer ratio, and the *TOPSwitch* control current to duty cycle transfer function set the DC control loop gain. C5 together with the control pin dynamic impedance and capacitor ESR establish a control loop pole-zero pair. C5 also determines the auto-restart frequency and filters internal gate drive switching currents. R2 and VR2 provide minimum current loading when output current is low. See DN-11 for more information regarding low-cost, 15 W power supplies.

Accurate Optocoupler Feedback

The circuit shown in Figure 9 is a highly accurate, 15 V, 30 W secondary-regulated flyback power supply that will operate from 85 to 132 VAC input voltage. A TL431 shunt regulator directly senses and accurately regulates the output voltage. The effective output voltage can be fine tuned by adjusting the resistor divider formed by R4 and R5. Other output voltages are possible by adjusting the transformer turns ratios as well as the divider ratio.

The general operation of the input and power stages of this circuit are the same as that described for Figures 7 and 8. R3 and C5 tailor frequency response. The TL431 (U3) regulates the output voltage by controlling optocoupler LED current (and *TOPSwitch* duty cycle) to maintain an average voltage of 2.5 V at the TL431 input pin. Divider R4 and R5 determine the actual output voltage. C9 rolls off the high frequency gain of the TL431 for stable operation. R1 limits optocoupler LED current and determines high frequency loop gain. For more information, refer to application note AN-14.

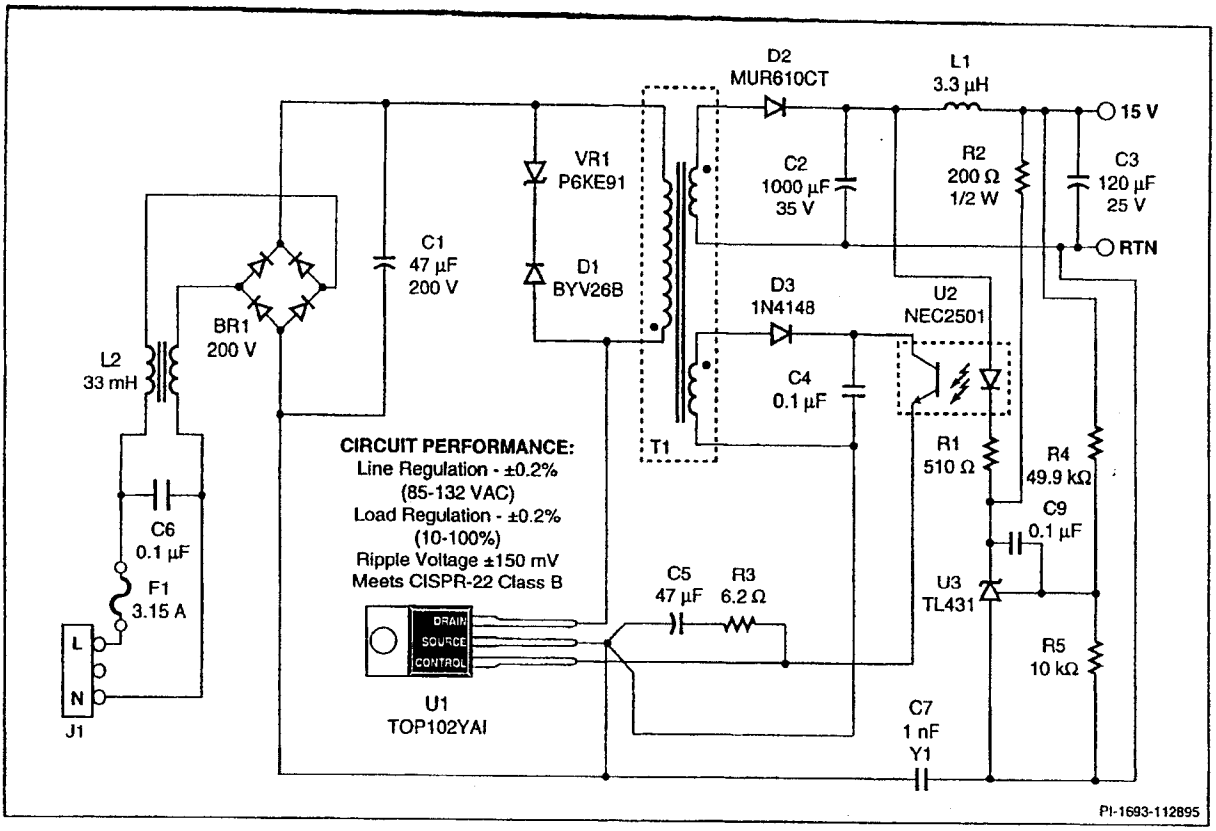


Figure 9. Schematic Diagram of a 30 W 100/110 VAC Input Power Supply Utilizing the TOP102 and Accurate Optocoupler Feedback.

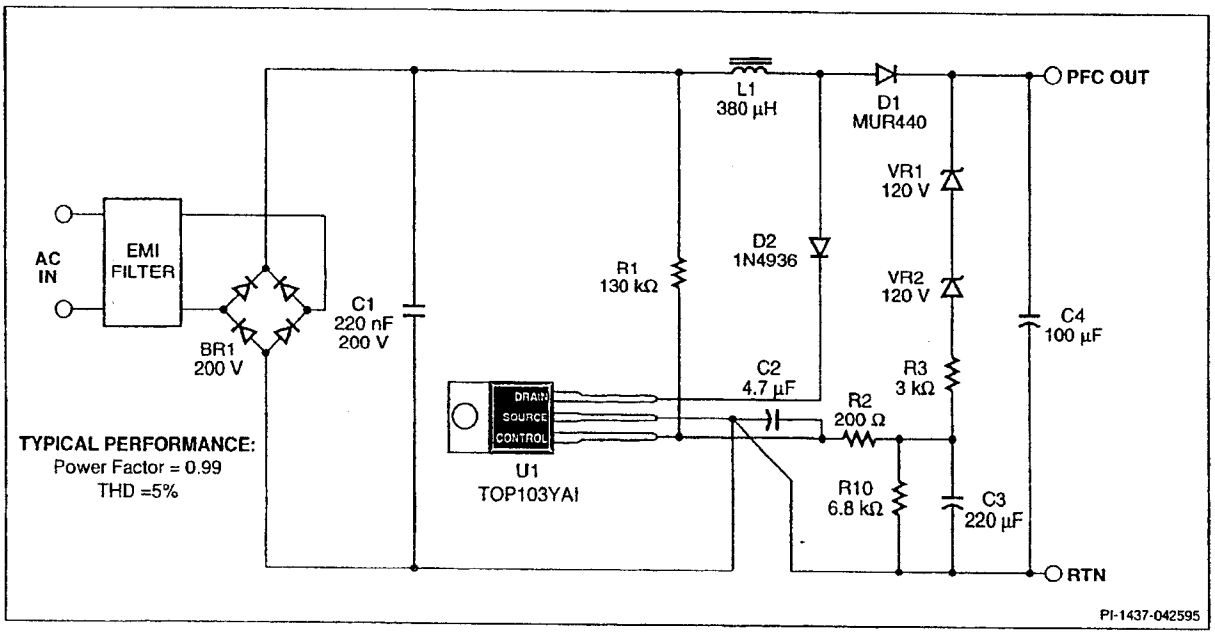


Figure 10. Schematic Diagram of a 60 W 110 VAC Input Boost Power Factor Correction Circuit Utilizing the TOP103.

General Circuit Operation (cont.)

Boost PFC Pre-regulator

TOPSwitch can also be used as a fixed frequency, discontinuous mode boost pre-regulator to improve Power Factor and reduce Total Harmonic Distortion (THD) for applications such as power supplies and electronic ballasts. The circuit shown in Figure 10 operates from 110 VAC and delivers 60 W at 265 VDC with typical Power Factor over 0.99 and THD of 5%. Bridge Rectifier BR1 full wave rectifies the AC input voltage. L1, D1, C4, and *TOPSwitch* make up the boost power stage. D2 prevents reverse current through the *TOPSwitch* body diode due to ringing voltages generated by the boost inductance and parasitic capacitance. R1 generates a pre-compensation current proportional to the instantaneous rectified AC input voltage which directly varies the duty cycle. C2 filters high frequency switching currents while having no filtering effect on the line frequency pre-compensation current. R2 decouples the pre-compensation current from the large filter capacitor C3 to prevent an averaging effect which would increase total harmonic distortion. C1 filters high frequency noise currents which could cause errors in the pre-compensation current.

When power is first applied, C3 charges to typically 5.7 volts before *TOPSwitch* starts. C3 then provides *TOPSwitch* bias current until the output voltage becomes regulated. When the output voltage becomes regulated, series connected Zener diodes VR1 and VR2 begin to conduct, drive current into the *TOPSwitch* control pin, and directly control the duty cycle. C3 together with R3 perform low pass filtering on the feedback signal to prevent output line frequency ripple voltage from varying the duty cycle. For more information, refer to Design Note DN-7.

Key Application Issues

Keep the SOURCE pin length very short. Use a Kelvin connection to the SOURCE pin for the CONTROL pin bypass capacitor. Use single point grounding techniques at the SOURCE pin as shown in Figure 11.

Minimize peak voltage and ringing on the DRAIN voltage at turn-off. Use a Zener or TVS Zener diode to clamp the DRAIN voltage.

Do not plug the *TOPSwitch* device into a "hot" IC socket during test. External CONTROL pin capacitance may deliver a surge current sufficient to trigger the shutdown latch which turns the *TOPSwitch* off.

Under some conditions, externally provided bias or supply current driven into the CONTROL pin can hold the *TOPSwitch* in one of the 8 auto-restart cycles indefinitely and prevent starting. Shorting the CONTROL pin to the SOURCE pin will reset the *TOPSwitch*. To avoid this problem when doing bench evaluations, it is recommended that the V_C power supply be turned on before the DRAIN voltage is applied.

CONTROL pin currents during auto-restart operation are much lower at low input voltages (< 20 V) which increases the auto-restart cycle period (see the I_C vs. Drain Voltage Characteristic curve).

Short interruptions of AC power may cause *TOPSwitch* to enter the 8-count auto-restart cycle before starting again. This is because the input energy storage capacitors are not completely discharged and the CONTROL pin capacitance has not discharged below the pin internal power-up reset voltage.

In some cases, minimum loading may be necessary to keep a lightly loaded or unloaded output voltage within the desired range due to the minimum ON-time.

For additional applications information regarding the *TOPSwitch* family, refer to AN-14.

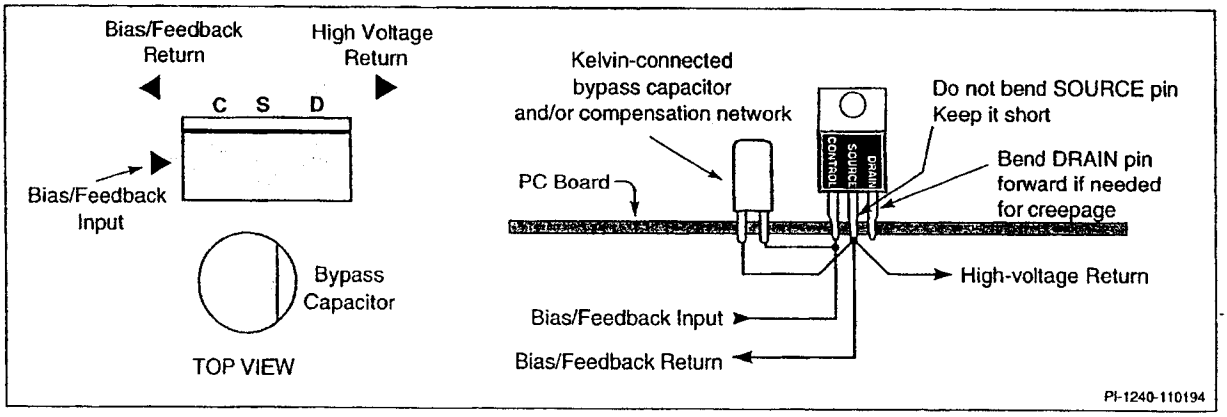


Figure 11. Recommended TOPSwitch Layout.

ABSOLUTE MAXIMUM RATINGS[1]

DRAIN Voltage ..... -0.3 to 350 V
CONTROL Voltage ..... - 0.3 V to 9 V
Storage Temperature ..... -65 to 125°C
Operating Junction Temperature[2] ..... -40 to 150°C
Lead Temperature[3] ..... 260°C

Thermal Impedance (θ_{JA}) ..... 70°C/W
Thermal Impedance (θ_{JC})[4] ..... 2 °C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C.
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.
4. Measured at tab closest to plastic interface.

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V T_j = -40 to 125°C		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	I_C = 4 mA, T_j = 25°C		90	100	110	kHz
Maximum Duty Cycle	DC_{MAX}	$I_C = I_{CD1}$ + 0.5 mA, See Figure 12		64	67	70	%
Minimum Duty Cycle	DC_{MIN}	I_C = 10 mA, See Figure 12		1.0	1.8	3.0	%
PWM Gain		I_C = 4 mA, T_j = 25°C See Figure 4		-11	-16	-21	%/mA
PWM Gain Temperature Drift		See Note 1			-0.05		%/mA/°C
External Bias Current	I_B	See Figure 4		1.5	2.5	4	mA
Dynamic Impedance	Z_C	I_C = 4 mA, T_j = 25°C See Figure 13		10	15	22	Ω
Dynamic Impedance Temperature Drift					0.18		%/°C
SHUTDOWN/AUTO-RESTART							
CONTROL Pin Charging Current	I_C	T_j = 25°C	V_C = 0 V	-2.4	-1.9	-1.2	mA
			V_C = 5 V	-2	-1.5	-0.8	
Charging Current Temperature Drift		See Note 1			0.4		%/°C
Auto-restart Threshold Voltage	$V_{C(AR)}$	S1 open			5.7		V

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V T_J = -40 to 125°C	Min	Typ	Max	Units
SHUTDOWN/AUTO-RESTART (cont.)						
UV Lockout Threshold Voltage		S1 open		4.7		V
Auto-restart Hysteresis Voltage		S1 open	0.6	1.0		V
Auto-restart Duty Cycle		S1 open		5	8	%
Auto-restart Frequency		S1 open		1.2		Hz
CIRCUIT PROTECTION						
Self-protection Current Limit	I_{LIMIT}	TOP100 di/dt = 160 mA/µs, T_J = 25°C	0.88		1.25	A
		TOP101 di/dt = 280 mA/µs, T_J = 25°C	1.50		2.15	
		TOP102 di/dt = 400 mA/µs, T_J = 25°C	2.20		3.10	
		TOP103 di/dt = 520 mA/µs, T_J = 25°C	2.85		4.00	
		TOP104 di/dt = 600 mA/µs, T_J = 25°C	3.30		4.60	
Leading Edge Blanking Time	t_{LEB}	I_C = 4 mA		150		ns
Current Limit Delay	t_{ILD}	I_C = 4 mA		100		ns
Thermal Shutdown Temperature		I_C = 4 mA	125	145		°C
Latched Shutdown Trigger Current	I_{SD}	See Figure 13	25	45	75	mA
Power-up Reset Threshold Voltage	$V_{C(RESET)}$	S2 open	2.0	3.3	4.2	V

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V T_J = -40 to 125°C		Min	Typ	Max	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	TOP100 I_D = 110 mA	T_J = 25°C		6.4	7.5	Ω
			T_J = 100°C		10.5	12.4	
		TOP101 I_D = 190 mA	T_J = 25°C		3.6	4.3	
			T_J = 100°C		6.0	7.1	
		TOP102 I_D = 270 mA	T_J = 25°C		2.6	3.0	
			T_J = 100°C		4.2	5.0	
		TOP103 I_D = 350 mA	T_J = 25°C		2.0	2.4	
			T_J = 100°C		3.3	3.9	
		TOP104 I_D = 400 mA	T_J = 25°C		1.7	2.0	
			T_J = 100°C		2.8	3.3	
OFF-State Current	I_{DSS}	Device in Latched Shutdown I_C = 4 mA, V_{DS} = 280 V, T_A = 125°C				500	µA
Breakdown Voltage	BV_{DSS}	Device in Latched Shutdown I_C = 4 mA, I_D = 500 µA, T_A = 25°C		350			V
Rise Time	t_r	Measured With Figure 8 Schematic			100		ns
Fall Time	t_f	Measured With Figure 8 Schematic			50		ns
SUPPLY							
DRAIN Supply Voltage		See Note 2		36			V
Shunt Regulator Voltage	$V_{C(SHUNT)}$	I_C = 4 mA		5.5	5.8	6.1	V
Shunt Regulator Temperature Drift					±50		ppm/°C
CONTROL Supply/ Discharge Current	I_{CD1}	Output MOSFET Enabled		0.6	1.2	1.6	mA
	I_{CD2}	Output MOSFET Disabled		0.5	0.8	1.1	

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 VS2 = 16 V R1 = 0 Ω SOURCE = 0 V T_J = -40 to 125°C		Min	Typ	Max	Units
LOW INPUT VOLTAGE OPERATION (See Note 3)							
DRAIN Supply Voltage		See Note 4		16			Volts
CONTROL Pin Charging Current		T_j = 25°C	V_C = 0 V	-2.3	-1.65	-1	mA
			V_C = 5 V	-1.2	-0.64	-0.28	mA
Auto-restart Duty Cycle		S1/Open			4	8	%
Auto-restart Frequency		S1/Open			0.85		Hz

NOTES:

1. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

2. It is possible to start up and operate *TOPSwitch* at DRAIN voltages well below 36 V. Refer to the "Low Input Voltage" Specification section for details.

3. This section specifies only parameters affected by low input voltage operation (Drain Voltages less than 36 V). All other parameters remain unchanged.

4. For low input voltage applications, the primary peak current could be set to a lower value than the current limit to increase efficiency. Refer to the Output Characteristics graph (Drain Current vs. Drain Voltage). The voltage across the transformer primary during the ON time is the difference between the input voltage and the drain voltage ($V_{DS(ON)}$).

   For example, if the input voltage is 16 VDC and a TOP104 (3.3A minimum current limit) is used at a primary peak current of 1A. Then the ($V_{DS(ON)}$) is 3 V at 100°C and the energizing voltage across the transformer primary is 13 V.

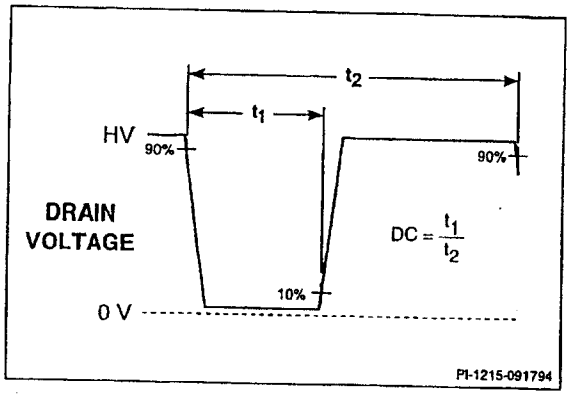


Figure 12. TOPSwitch Duty Cycle Measurement.

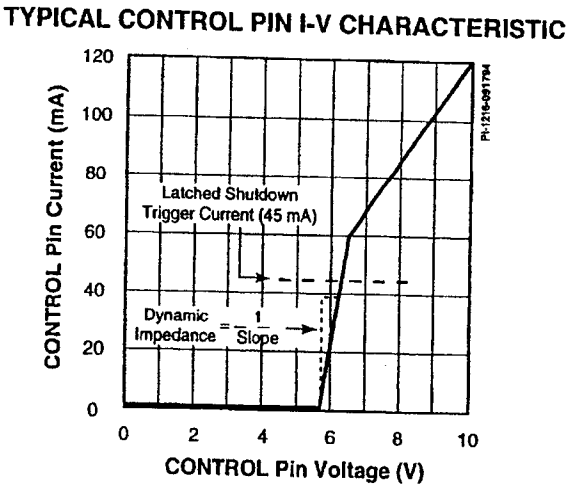


Figure 13. TOPSwitch CONTROL Pin I-V Characteristic.

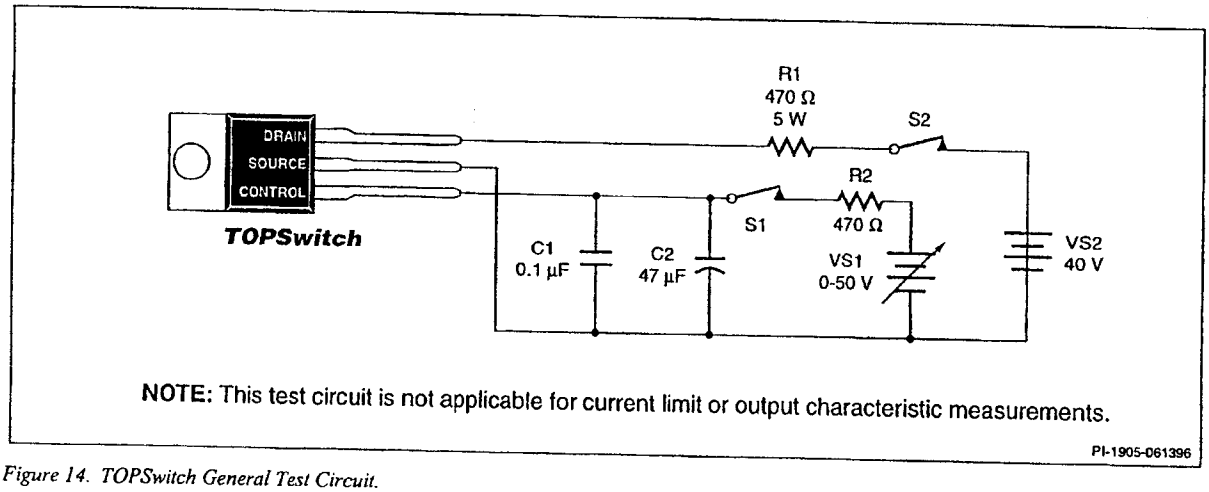


Figure 14. TOPSwitch General Test Circuit.

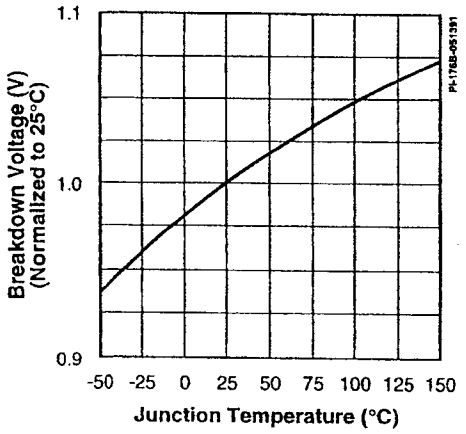
BENCH TEST PRECAUTIONS FOR EVALUATION OF ELECTRICAL CHARACTERISTICS

The following precautions should be followed when testing *TOPSwitch* by itself outside of a power supply. The schematic shown in Figure 14 is suggested for laboratory testing of *TOPSwitch*.

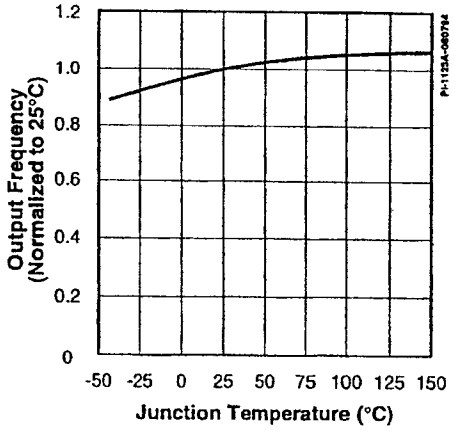
When the DRAIN supply is turned on, the part will be in the auto-restart mode. The control pin voltage will be oscillating at a low frequency from 4.7 to 5.7 V and the DRAIN is turned on every eighth cycle of the CONTROL pin oscillation. If the CONTROL pin power supply is turned on while in this auto-restart mode, there is only a 12.5% chance that the control pin oscillation will be in the correct state (DRAIN active state) so that the continuous DRAIN voltage waveform may be observed. It is recommended that the V_C power supply be turned on first and the DRAIN power supply second if continuous drain voltage waveforms are to be observed. The 12.5% chance of being in the correct state is due to the 8:1 counter.

Typical Performance Characteristics

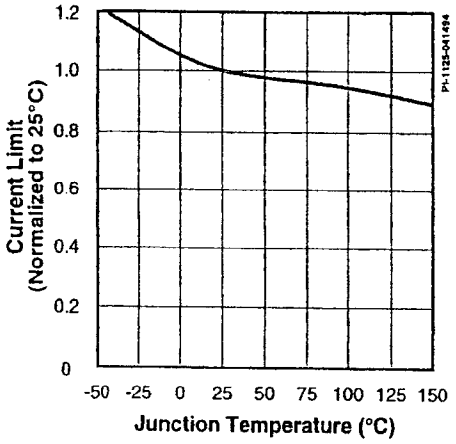
BREAKDOWN vs. TEMPERATURE



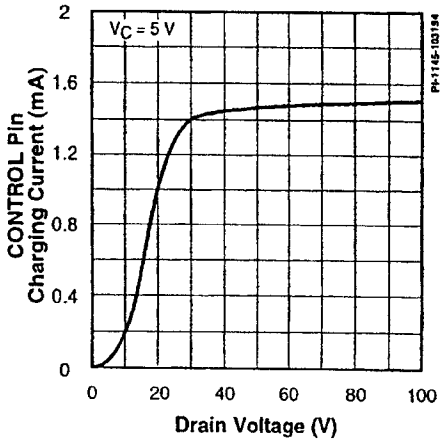
FREQUENCY vs. TEMPERATURE



CURRENT LIMIT vs. TEMPERATURE



I_C vs. DRAIN VOLTAGE



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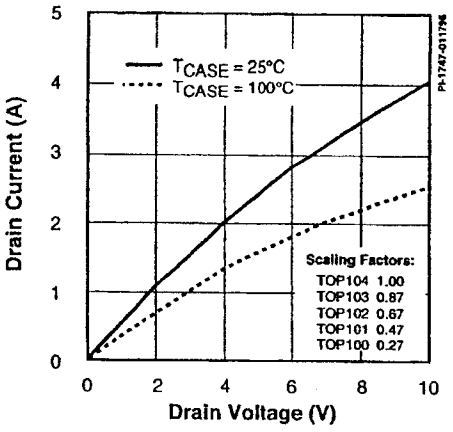
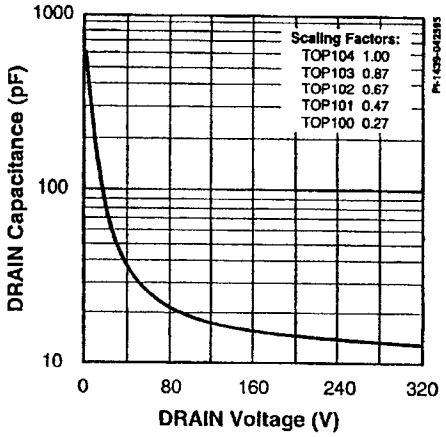
Typical Performance Characteristics (cont.)

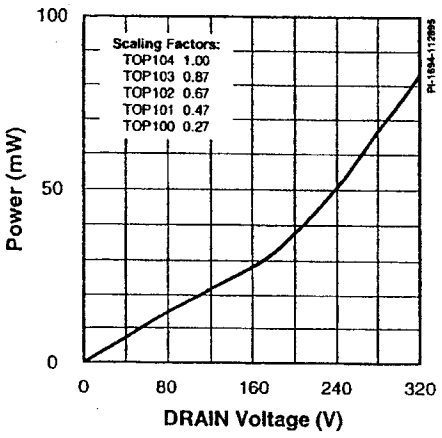
OUTPUT CHARACTERISTICS



COSS vs. DRAIN VOLTAGE



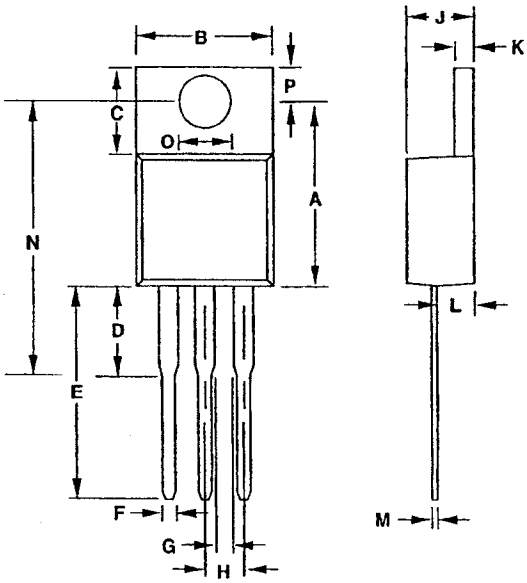
DRAIN CAPACITANCE POWER



Y03A — Plastic TO-220/3

DIM	Inches	mm
A	.460-.480	11.68-12.19
B	.400-.415	10.16-10.54
C	.236-.260	5.99-6.60
D	.240 - REF.	6.10 - REF.
E	.520-.560	13.21-14.22
F	.028-.038	.71-.97
G	.045-.055	1.14-1.40
H	.090-.110	2.29-2.79
J	.165-.185	4.19-4.70
K	.045-.055	1.14-1.40
L	.095-.115	2.41-2.92
M	.015-.020	.38-.51
N	.705-.715	17.91-18.16
O	.146-.156	3.71-3.96
P	.103-.113	2.62-2.87

* LEADS AND TAB ARE SOLDER PLATED



Notes:
1. Package dimensions conform to JEDEC specification TO-220 AB for standard flange mounted, peripheral lead package; .100 inch lead spacing (Plastic) 3 leads (Issue J, March 1987)
2. Controlling dimensions are inches.
3. Pin numbers start with Pin 1, and continue from left to right when viewed from the top.
4. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15 mm) on any side.
5. Position of terminals to be measured at a position .25 (6.35 mm) from the body.
6. All terminals are solder plated.

PI-1848-050696

NOTES

NOTES

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EXHIBIT B

TOP200-4/14

TOPSwitch® Family

Three-terminal Off-line PWM Switch

POWER INTEGRATIONS, INC.®

Product Highlights

Low Cost Replacement for Discrete Switchers
- 20 to 50 fewer components - cuts cost, increases reliability
- Source-connected tab and Controlled MOSFET turn-on reduce EMI and EMI filter costs
- Allows for a 50% smaller and lighter solution
- Cost competitive with linears above 5 W

Up to 90% Efficiency in Flyback Topology
- Built-in start-up and current limit reduce DC losses
- Low capacitance 700 V MOSFET cuts AC losses
- CMOS controller/gate driver consumes only 6 mW
- 70% maximum duty cycle minimizes conduction losses

Simplifies Design - Reduces Time to Market
- Supported by many reference design boards
- Integrated PWM Controller and 700 V MOSFET in a industry standard three pin TO-220 package
- Only one external capacitor needed for compensation, bypass and start-up/auto-restart functions

System Level Fault Protection Features
- Auto-restart and cycle by cycle current limiting functions handle both primary and secondary faults
- On-chip latching thermal shutdown protects the entire system against overload

Highly Versatile
- Implements Buck, Boost, Flyback or Forward topology
- Easily interfaces with both opto and primary feedback
- Supports continuous or discontinuous mode of operation

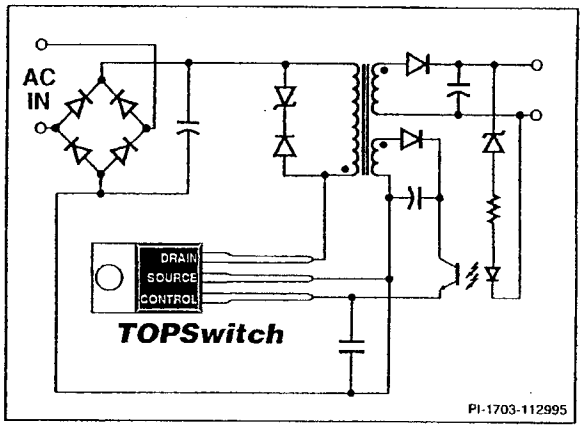


Figure 1. Typical Application.

TOPSwitch SELECTION GUIDE			
ORDER PART NUMBER	OUTPUT POWER RANGE		
	FLYBACK		PFC/ BOOST
	230 VAC or 110 VAC w/Doubler	85-265 VAC	230/277 VAC
TOP200YAI*	0-25 W	0-12 W	0-25 W
TOP201YAI*	20-45 W	10-22 W	20-50 W
TOP202YAI*	30-60 W	15-30 W	30-75 W
TOP203YAI*	40-70 W	20-35 W	50-100 W
TOP214YAI*	50-85 W	25-42 W	60-125 W
TOP204YAI*	60-100 W	30-50 W	75-150 W

* Package Outline: Y03A

Description

The *TOPSwitch* family implements, with only three pins, all functions necessary for an off-line switched mode control system: high voltage N-channel power MOSFET with controlled turn-on gate driver, voltage mode PWM controller with integrated 100 kHz oscillator, high voltage start-up bias circuit, bandgap derived reference, bias shunt regulator/error amplifier for loop compensation and fault protection circuitry. Compared to discrete MOSFET and controller or self oscillating (RCC) switching converter solutions, a *TOPSwitch* integrated circuit can reduce total cost, component count, size, weight and at the same time increase efficiency and system reliability. These devices are intended for 100/110/230 VAC off-line Power Supply applications in the 0 to 100 W (0 to 50 W universal) range and 230/277 VAC off-line power factor correction (PFC) applications in the 0 to 150 W range.

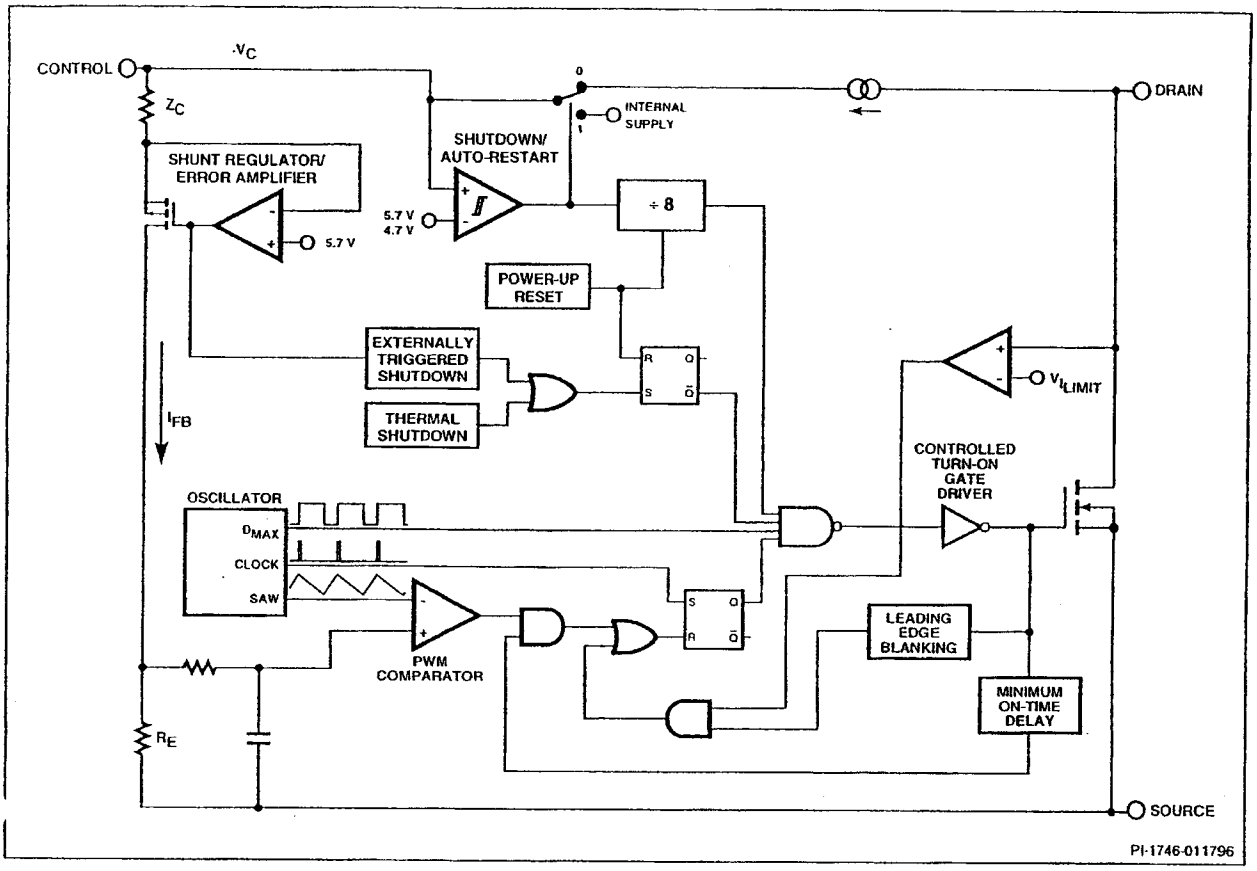


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN Pin:
Output MOSFET drain connection. Provides internal bias current during start-up operation via an internal switched high-voltage current source. Internal current sense point.

CONTROL Pin:
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. Trigger input for latching shutdown. It is also used as the supply bypass and auto-restart/ compensation capacitor connection point.

SOURCE Pin:
Output MOSFET source connection. Primary-side circuit common, power return, and reference point.

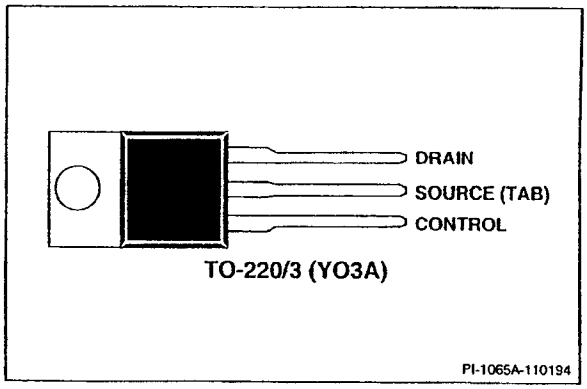


Figure 3. Pin Configuration.

TOPSwitch Family Functional Description

TOPSwitch is a self biased and protected linear control current-to-duty cycle converter with an open drain output. High efficiency is achieved through the use of CMOS and integration of the maximum number of functions possible. CMOS significantly reduces bias currents as compared to bipolar or discrete solutions. Integration eliminates external power resistors used for current sensing and/or supplying initial start-up bias current.

During normal operation, the internal output MOSFET duty cycle linearly decreases with increasing CONTROL pin current as shown in Figure 4. To implement all the required control, bias, and protection functions, the DRAIN and CONTROL pins each perform several functions as described below. Refer to Figure 2 for a block diagram and Figure 6 for timing and voltage waveforms of the *TOPSwitch* integrated circuit.

Control Voltage Supply

CONTROL pin voltage V_C is the supply or bias voltage for the controller and driver circuitry. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the gate drive current. The total amount of capacitance connected to this pin (C_T) also sets the auto-restart timing as well as control loop compensation. V_C is regulated in either of two modes of operation. Hysteretic regulation is used for initial start-up and overload operation. Shunt regulation is used to separate the duty cycle error signal from the control circuit supply current. During start-up, V_C current is supplied from a high-voltage switched current source connected internally between the DRAIN and CONTROL pins. The current source provides sufficient current to supply the control circuitry as well as charge the total external capacitance (C_T).

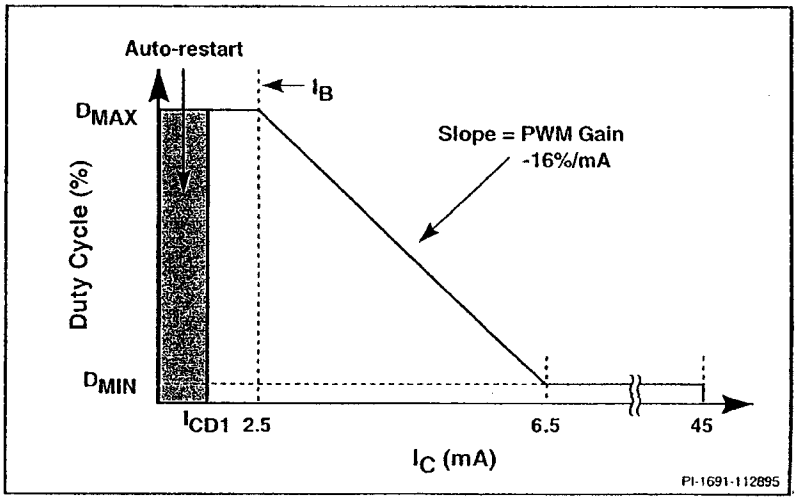


Figure 4. Relationship of Duty Cycle to CONTROL Pin Current.

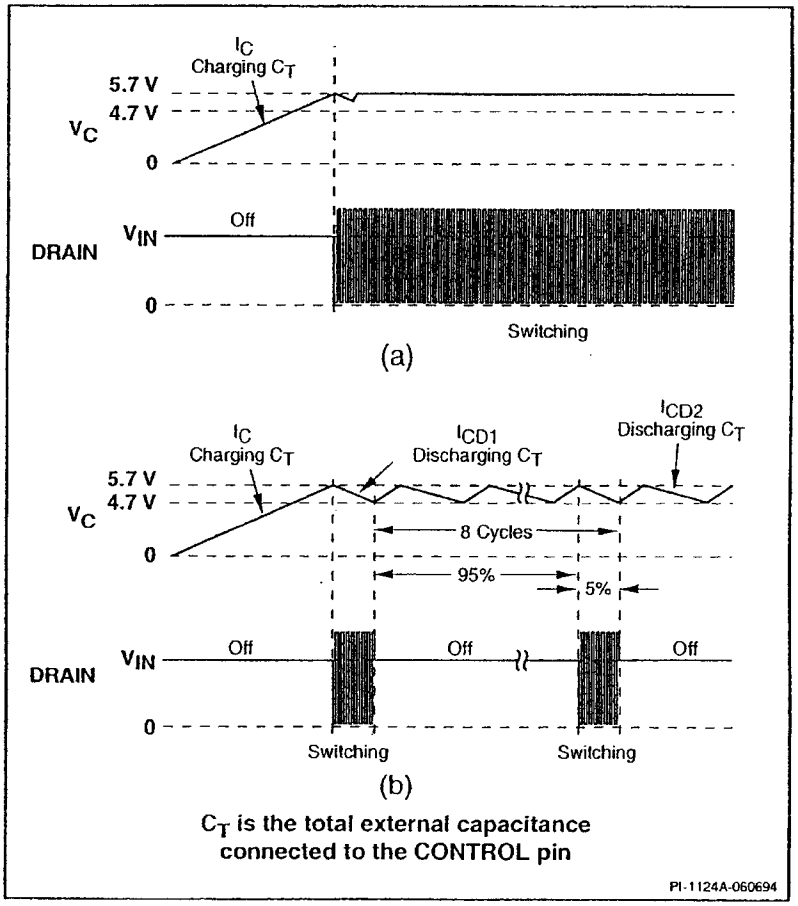


Figure 5. Start-up Waveforms for (a) Normal Operation and (b) Auto-restart.

TOPSwitch Family Functional Description (cont.)

The first time V_C reaches the upper threshold, the high-voltage current source is turned off and the PWM modulator and output transistor are activated, as shown in Figure 5(a). During normal operation (when the output voltage is regulated) feedback control current supplies the V_C supply current. The shunt regulator keeps V_C at typically 5.7 V by shunting CONTROL pin feedback current exceeding the required DC supply current through the PWM error signal sense resistor R_E. The low dynamic impedance of this pin (Z_C) sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance of the CONTROL pin together with the external resistance and capacitance determines the control loop compensation of the power system.

If the CONTROL pin external capacitance (C_T) should discharge to the lower threshold, then the output MOSFET is turned off and the control circuit is placed in a low-current standby mode. The high-voltage current source is turned on and charges the external capacitance again. Charging current is shown with a negative polarity and discharging current is shown with a positive polarity in Figure 6. The hysteretic auto-restart comparator keeps V_C within a window of typically 4.7 to 5.7 V by turning the high-voltage current source on and off as shown in Figure 5(b). The auto-restart circuit has a divide-by-8 counter which prevents the output MOSFET from turning on again until eight discharge-charge cycles have elapsed. The counter effectively limits *TOPSwitch* power dissipation by reducing the auto-restart duty cycle to typically 5%. Auto-restart continues to cycle until output voltage regulation is again achieved.

Bandgap Reference

All critical *TOPSwitch* internal voltages are derived from a temperature-compensated bandgap reference. This reference is also used to generate a temperature-compensated current source which is trimmed to accurately set the oscillator frequency and MOSFET gate drive current.

Oscillator

The internal oscillator linearly charges and discharges the internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle. The nominal frequency of 100 kHz was chosen to minimize EMI and maximize efficiency in power supply applications. Trimming of the current reference improves oscillator frequency accuracy.

Pulse Width Modulator

The pulse width modulator implements a voltage-mode control loop by driving the output MOSFET with a duty cycle inversely proportional to the current flowing into the CONTROL pin. The error signal across R_E is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise. The filtered error signal is compared with the internal oscillator sawtooth waveform to generate the duty cycle waveform. As the control current increases, the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the output MOSFET. The pulse width modulator resets the latch, turning off the output MOSFET. The maximum duty cycle is set by the symmetry of the internal oscillator. The modulator has a minimum ON-time to keep the current consumption of the *TOPSwitch* independent of the error signal. Note that a minimum current must be driven into the CONTROL pin before the duty cycle begins to change.

Gate Driver

The gate driver is designed to turn the output MOSFET on at a controlled rate to minimize common-mode EMI. The gate drive current is trimmed for improved accuracy.

Error Amplifier

The shunt regulator can also perform the function of an error amplifier in primary feedback applications. The shunt regulator voltage is accurately derived from the temperature compensated bandgap reference. The gain of the error amplifier is set by the CONTROL pin dynamic impedance. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and flows through R_E as the error signal.

Cycle-By-Cycle Current Limit

The cycle by cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET ON-state drain-source voltage, $V_{DS(ON)}$, with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize variation of the effective peak current limit due to temperature related changes in output MOSFET $R_{DS(ON)}$.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that current spikes caused by primary-side capacitances and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

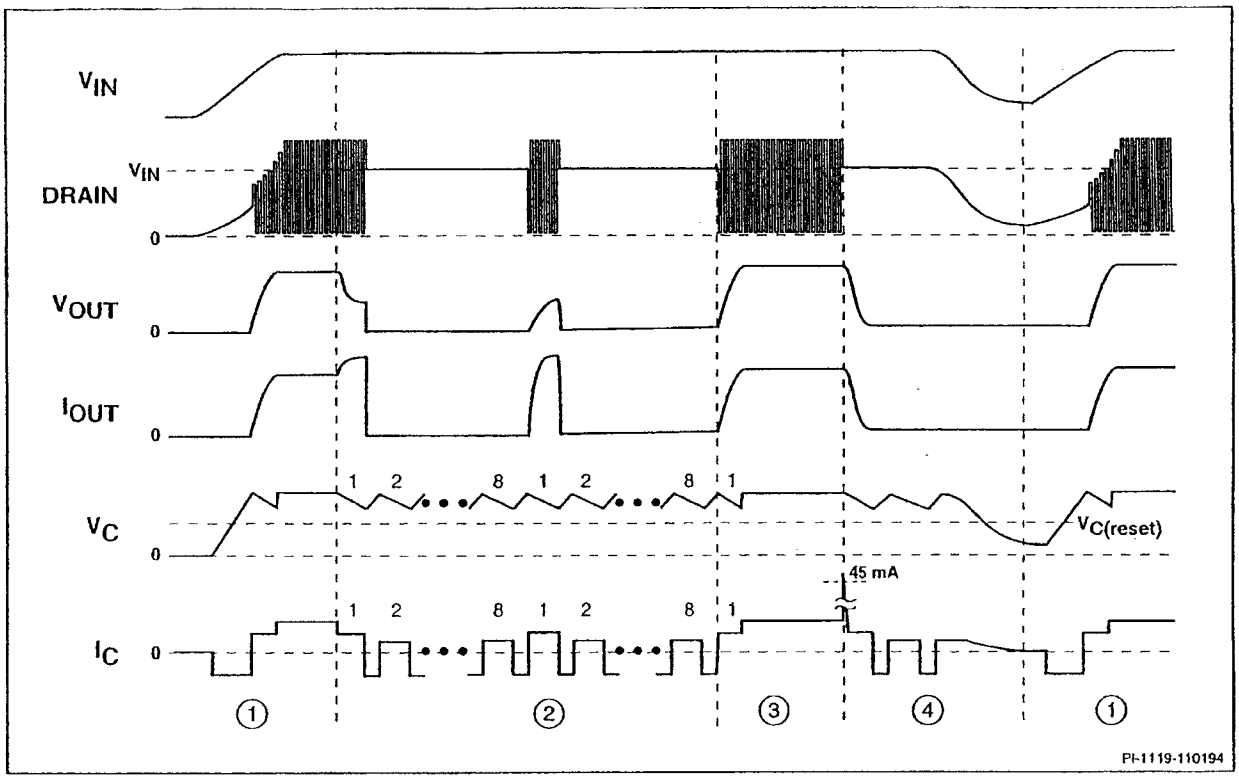


Figure 6. Typical Waveforms for (1) Normal Operation, (2) Auto-restart, (3) Latching Shutdown, and (4) Power Down Reset.

Shutdown/Auto-restart

To minimize *TOPSwitch* power dissipation, the shutdown/auto-restart circuit turns the power supply on and off at a duty cycle of typically 5% if an out of regulation condition persists. Loss of regulation interrupts the external current into the CONTROL pin. V_C regulation changes from shunt mode to the hysteretic auto-restart mode described above. When the fault condition is removed, the power supply output becomes regulated, V_C regulation returns to shunt mode, and normal operation of the power supply resumes.

Latching Shutdown

The output overvoltage protection latch is activated by a high-current pulse into the CONTROL pin. When set, the latch turns off the *TOPSwitch* output. Activating the power-up reset circuit by removing and restoring input power, or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. V_C is regulated in hysteretic mode when the power supply is latched off.

Overtemperature Protection

Temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (typically 145°C). Activating the power-up reset circuit by removing and restoring input power or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. V_C is regulated in hysteretic mode when the power supply is latched off.

High-voltage Bias Current Source

This current source biases *TOPSwitch* from the DRAIN pin and charges the CONTROL pin external capacitance (C_T) during start-up or hysteretic operation. Hysteretic operation occurs during auto-restart and latched shutdown. The current source is switched on and off with an effective duty cycle of approximately 35%. This duty cycle is determined by the ratio of CONTROL pin charge (I_C) and discharge currents (I_{CD1} and I_{CD2}). This current source is turned off during normal operation when the output MOSFET is switching.

General Circuit Operation

Primary Feedback Regulation

The circuit shown in Figure 7 is a simple 5 V, 5 W bias supply using the TOP200. This universal input flyback power supply employs primary-side regulation from a transformer bias winding. This approach is best for low-cost applications requiring isolation and operation within a narrow range of load variation. Line and load regulation of ±5% or better can be achieved from 10% to 100% of rated load.

Voltage feedback is obtained from the transformer (T1) bias winding, which eliminates the need for optocoupler and secondary-referenced error amplifier. High-voltage DC is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated high-voltage MOSFET transistor within the TOP200 (U1). The circuit operates at a switching frequency of 100 kHz, set by the internal oscillator of the TOP200. The clamp circuit implemented by VR1 and D1 limits the leading-edge voltage spike caused by transformer leakage inductance to a safe value. The 5 V power secondary winding is rectified and filtered by D2, C2, C3, and L1 to create the 5 V output voltage.

The output of the T1 bias winding is rectified and filtered by D3, R1, and C5. The voltage across C5 is regulated by U1, and is determined by the 5.7 V internal shunt regulator at the CONTROL pin of U1. When the rectified bias voltage on C5 begins to exceed the shunt regulator voltage, current will flow into the control pin. Increasing control pin current decreases the duty cycle until a stable operating point is reached. The output voltage is proportional to the bias voltage by the turns ratio of the output to bias windings. C5 is used to bypass the CONTROL pin. C5 also provides loop compensation for the power supply by shunting AC currents around the CONTROL pin dynamic impedance, and also determines the auto-restart frequency during start-up and auto-restart conditions. See DN-8 for more information regarding the use of the TOP200 in bias supplies.

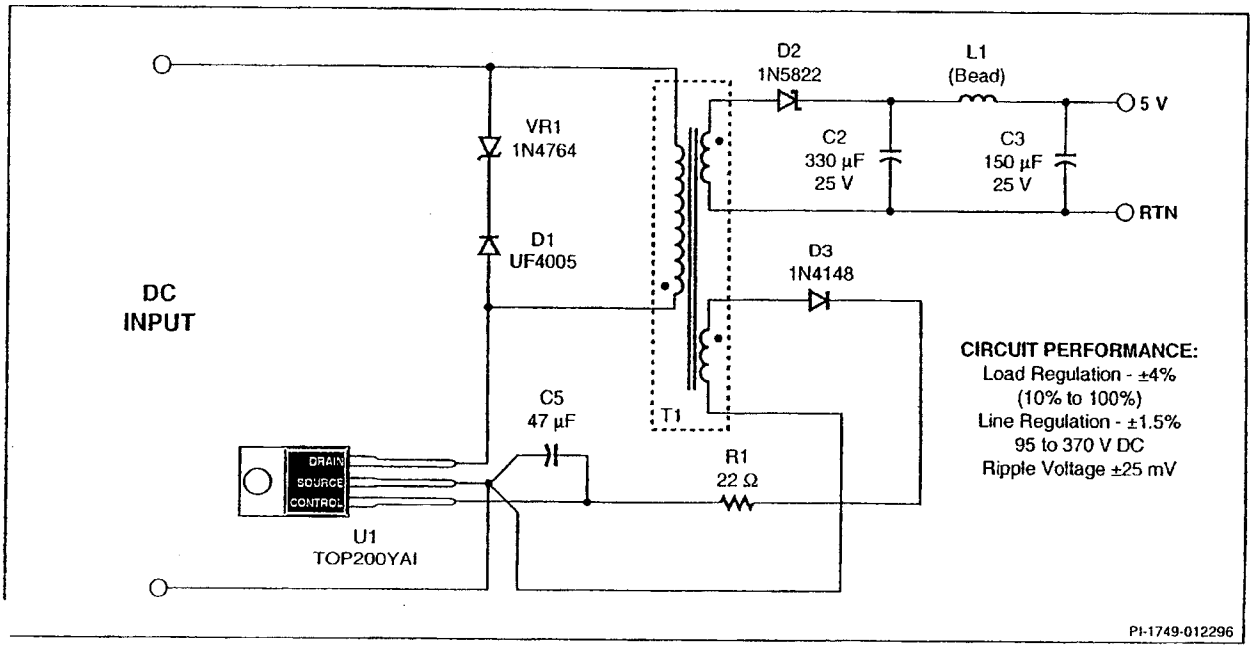


Figure 7. Schematic Diagram of a Minimum Parts Count 5 V, 5 W Bias Supply Utilizing the TOP200.

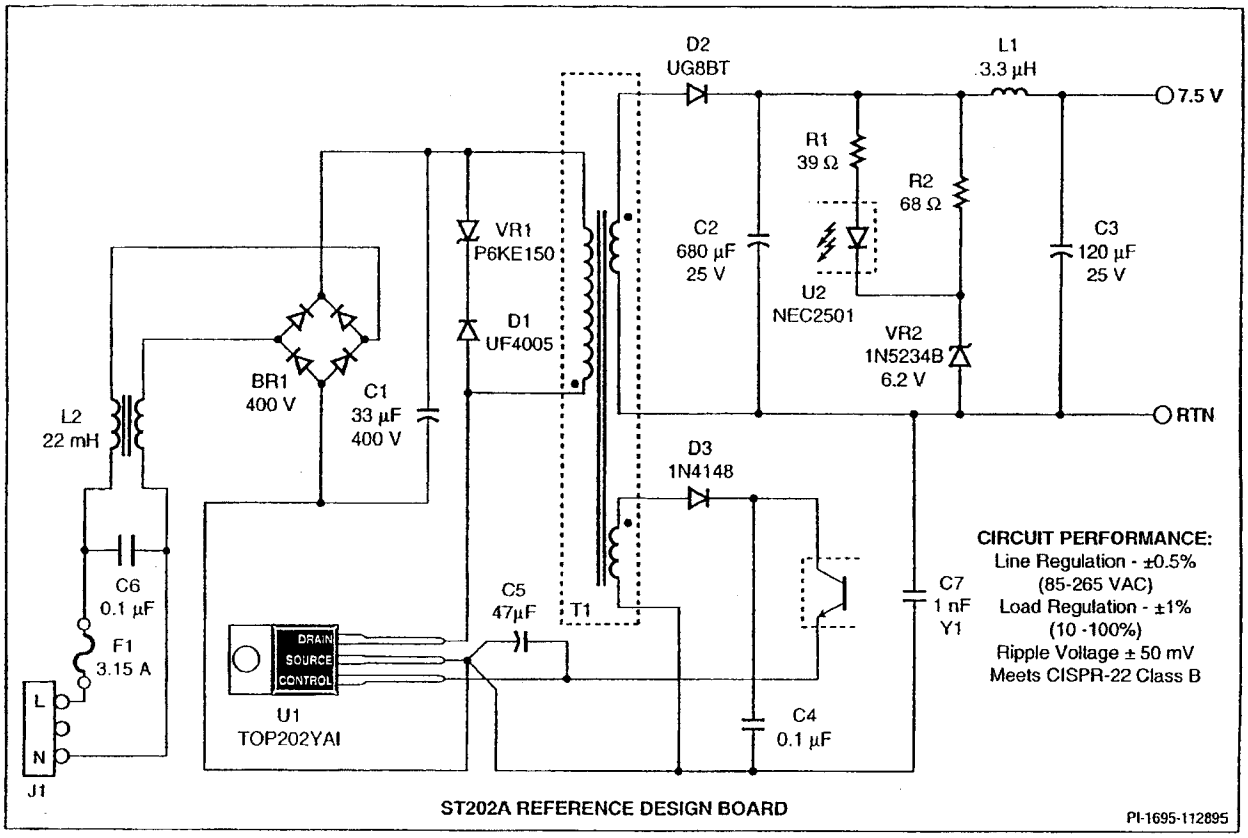


Figure 8. Schematic Diagram of a 15 W Universal Input Power Supply Utilizing the TOP202 and Simple Optocoupler Feedback.

Simple Optocoupler Feedback

The circuit shown in Figure 8 is a 7.5 V, 15 W secondary regulated flyback power supply using the TOP202 that will operate from 85 to 265 VAC input voltage. Improved output voltage accuracy and regulation over the circuit of Figure 7 is achieved by using an optocoupler and secondary referenced Zener diode. The general operation of the power stage of this circuit is the same as that described for Figure 7.

The input voltage is rectified and filtered by BR1 and C1. L2, C6 and C7 reduce conducted emission currents. The bias winding is rectified and filtered by D3 and C4 to create a typical 11 V bias voltage. Zener diode (VR2) voltage together with the forward voltage of the LED in the optocoupler U2 determine the output voltage. R1, the optocoupler current transfer ratio, and the *TOPSwitch* control current to duty cycle transfer function set the DC control loop gain. C5 together with the control pin dynamic impedance and capacitor ESR establish a control loop pole-zero pair. C5 also determines the auto-restart frequency and filters internal gate drive switching currents. R2 and VR2 provide minimum current loading when output current is low. See DN-11 for more information regarding the use of the TOP202 in a low-cost, 15 W universal power supply.

Accurate Optocoupler Feedback

The circuit shown in Figure 9 is a highly accurate, 15 V, 30 W secondary-regulated flyback power supply that will operate from 85 to 265 VAC input voltage. A TL431 shunt regulator directly senses and accurately regulates the output voltage. The effective output voltage can be fine tuned by adjusting the resistor divider formed by R4 and R5. Other output voltages are possible by adjusting the transformer turns ratios as well as the divider ratio..

The general operation of the input and power stages of this circuit are the same as that described for Figures 7 and 8. R3 and C5 tailor frequency response. The TL431 (U2) regulates the output voltage by controlling optocoupler LED current (and *TOPSwitch* duty cycle) to maintain an average voltage of 2.5 V at the TL431 input pin. Divider R4 and R5 determine the actual output voltage. C9 rolls off the high frequency gain of the TL431 for stable operation. R1 limits optocoupler LED current and determines high frequency loop gain. For more information, refer to application note AN-14.

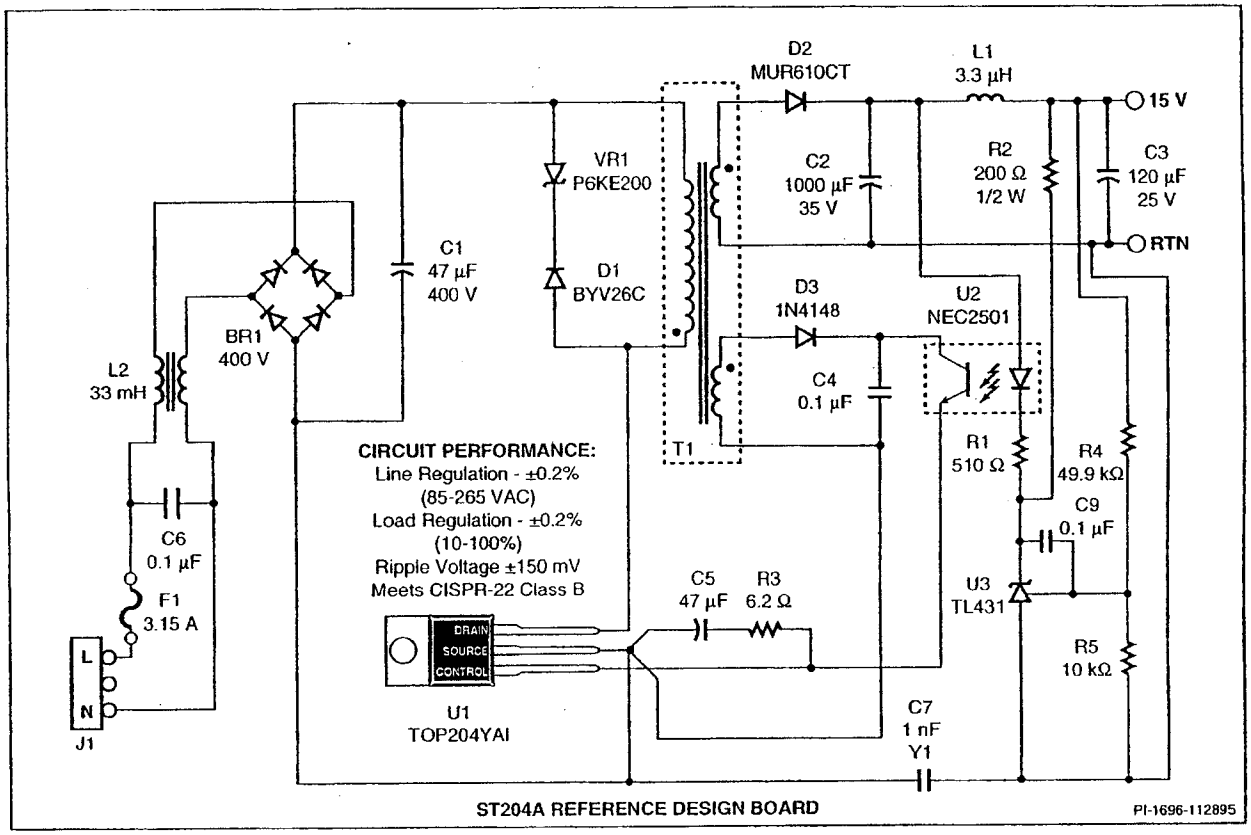


Figure 9. Schematic Diagram of a 30 W Universal Input Power Supply Utilizing the TOP204 and Accurate Optocoupler Feedback.

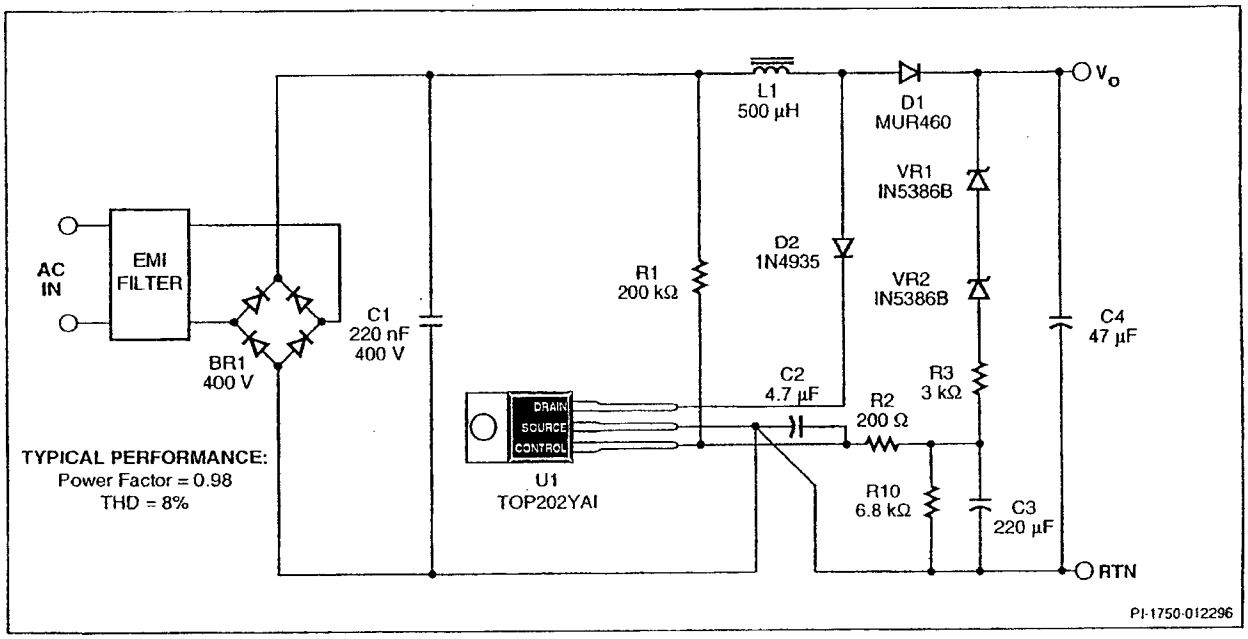


Figure 10. Schematic Diagram of a 65 W 230 VAC Input Boost Power Factor Correction Circuit Utilizing the TOP202.

General Circuit Operation (cont.)

Boost PFC Pre-regulator

TOPSwitch can also be used as a fixed frequency, discontinuous mode boost pre-regulator to improve Power Factor and reduce Total Harmonic Distortion (THD) for applications such as power supplies and electronic ballasts. The circuit shown in Figure 10 operates from 230 VAC and delivers 65 W at 410 VDC with typical Power Factor over 0.98 and THD of 8%. Bridge Rectifier BR1 full wave rectifies the AC input voltage. L1, D1, C4, and *TOPSwitch* make up the boost power stage. D2 prevents reverse current through the *TOPSwitch* body diode due to ringing voltages generated by the boost inductance and parasitic capacitance. R1 generates a pre-compensation current proportional to the instantaneous rectified AC input voltage which directly varies the duty cycle. C2 filters high frequency switching currents while having no filtering effect on the line frequency pre-compensation current. R2 decouples the pre-compensation current from the large filter capacitor C3 to prevent an averaging effect which would increase total harmonic distortion. C1 filters high frequency noise currents which could cause errors in the pre-compensation current.

When power is first applied, C3 charges to typically 5.7 volts before *TOPSwitch* starts. C3 then provides *TOPSwitch* bias current until the output voltage becomes regulated. When the output voltage becomes regulated, series connected Zener diodes VR1 and VR2 begin to conduct, drive current into the *TOPSwitch* control pin, and directly control the duty cycle. C3 together with R3 perform low pass filtering on the feedback signal to prevent output line frequency ripple voltage from varying the duty cycle. For more information, refer to Design Note DN-7.

Key Application Issues

Keep the SOURCE pin length very short. Use a Kelvin connection to the SOURCE pin for the CONTROL pin bypass capacitor. Use single point grounding techniques at the SOURCE pin as shown in Figure 11.

Minimize peak voltage and ringing on the DRAIN voltage at turn-off. Use a Zener or TVS Zener diode to clamp the DRAIN voltage.

Do not plug the *TOPSwitch* device into a "hot" IC socket during test. External CONTROL pin capacitance may deliver a surge current sufficient to trigger the shutdown latch which turns the *TOPSwitch* off.

Under some conditions, externally provided bias or supply current driven into the CONTROL pin can hold the *TOPSwitch* in one of the 8 auto-restart cycles indefinitely and prevent starting. Shorting the CONTROL pin to the SOURCE pin will reset the *TOPSwitch*. To avoid this problem when doing bench evaluations, it is recommended that the V_C power supply be turned on before the DRAIN voltage is applied.

CONTROL pin currents during auto-restart operation are much lower at low input voltages (< 20 V) which increases the auto-restart cycle period (see the I_C vs. Drain Voltage Characteristic curve).

Short interruptions of AC power may cause *TOPSwitch* to enter the 8-count auto-restart cycle before starting again. This is because the input energy storage capacitors are not completely discharged and the CONTROL pin capacitance has not discharged below the pin internal power-up reset voltage.

In some cases, minimum loading may be necessary to keep a lightly loaded or unloaded output voltage within the desired range due to the minimum ON-time.

For additional applications information regarding the *TOPSwitch* family, refer to AN-14.

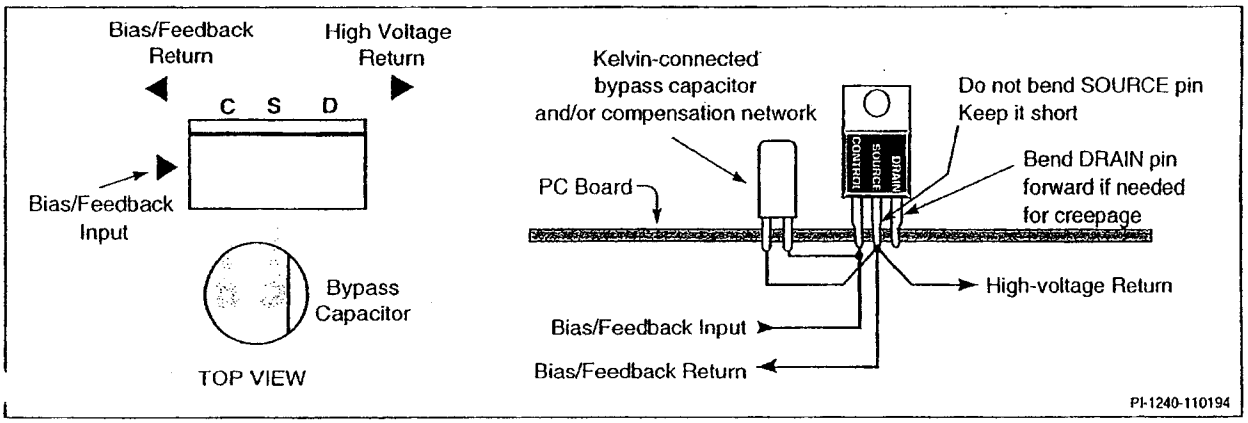


Figure 11. Recommended TOPSwitch Layout.

ABSOLUTE MAXIMUM RATINGS(1)

DRAIN Voltage ..... -0.3 to 700 V
CONTROL Voltage ..... - 0.3 V to 9 V
Storage Temperature ..... -65 to 125°C
Operating Junction Temperature(2) ..... -40 to 150°C
Lead Temperature(3) ..... 260°C

Thermal Impedance (θ_{JA}) ..... 70°C/W
Thermal Impedance (θ_{JC})(4) ..... 2 °C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C.
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.
4. Measured at tab closest to plastic interface.

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V T_j = -40 to 125°C		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	I_C = 4 mA, T_j = 25°C		90	100	110	kHz
Maximum Duty Cycle	DC_{MAX}	$I_C = I_{CD1}$ + 0.5 mA, See Figure 12		64	67	70	%
Minimum Duty Cycle	DC_{MIN}	I_C = 10 mA, See Figure 12	TOP200/1/2	1.0	1.8	3.0	%
			TOP203/4/14	1.0	2.0	3.5	
PWM Gain		I_C = 4 mA, T_j = 25°C See Figure 4		-11	-16	-21	%/mA
PWM Gain Temperature Drift		See Note 1			-0.05		%/mA/°C
External Bias Current	I_B	See Figure 4		1.5	2.5	4	mA
Dynamic Impedance	Z_C	I_C = 4 mA, T_j = 25°C See Figure 13		10	15	22	Ω
Dynamic Impedance Temperature Drift					0.18		%/°C
SHUTDOWN/AUTO-RESTART							
CONTROL Pin Charging Current	I_C	T_j = 25°C	V_C = 0 V	-2.4	-1.9	-1.2	mA
			V_C = 5 V	-2	-1.5	-0.8	
Charging Current Temperature Drift		See Note 1			0.4		%/°C
Auto-restart Threshold Voltage	$V_{C(AR)}$	S1 open			5.7		V

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V T_j = -40 to 125°C	Min	Typ	Max	Units
SHUTDOWN/AUTO-RESTART (cont.)						
UV Lockout Threshold Voltage		S1 open		4.7		V
Auto-restart Hysteresis Voltage		S1 open	0.6	1.0		V
Auto-restart Duty Cycle		S1 open		5	8	%
Auto-restart Frequency		S1 open		1.2		Hz
CIRCUIT PROTECTION						
Self-protection Current Limit	I_{LIMIT}	TOP200 di/dt = 80 mA/µs, T_j = 25°C	0.415		0.585	A
		TOP201 di/dt = 170 mA/µs, T_j = 25°C	0.830		1.17	
		TOP202 di/dt = 250 mA/µs, T_j = 25°C	1.25		1.75	
		TOP203 di/dt = 330 mA/µs, T_j = 25°C	1.50		2.10	
		TOP214 di/dt = 420 mA/µs, T_j = 25°C	1.88		2.63	
		TOP204 di/dt = 500 mA/µs, T_j = 25°C	2.25		3.15	
Leading Edge Blanking Time	t_{LEB}	I_C = 4 mA		150		ns
Current Limit Delay	t_{ILD}	I_C = 4 mA		100		ns
Thermal Shutdown Temperature		I_C = 4 mA	125	145		°C
Latched Shutdown Trigger Current	I_{SD}	See Figure 13	25	45	75	mA
Power-up Reset Threshold Voltage	$V_{C(RESET)}$	S2 open	2.0	3.3	4.2	V

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V T_j = -40 to 125°C		Min	Typ	Max	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	TOP200 I_D = 50 mA	T_j = 25°C		15.6	18.0	Ω
			T_j = 100°C		25.7	29.7	
		TOP201 I_D = 100 mA	T_j = 25°C		7.8	9.0	
			T_j = 100°C		12.9	14.9	
		TOP202 I_D = 150 mA	T_j = 25°C		5.2	6.0	
			T_j = 100°C		8.6	9.9	
		TOP203 I_D = 200 mA	T_j = 25°C		3.9	4.5	
			T_j = 100°C		6.4	7.5	
		TOP214 I_D = 250 mA	T_j = 25°C		3.1	3.6	
			T_j = 100°C		5.2	6.0	
		TOP204 I_D = 300 mA	T_j = 25°C		2.6	3.0	
			T_j = 100°C		4.3	5.0	
OFF-State Current	I_{DSS}	Device in Latched Shutdown I_C = 4 mA, V_{DS} = 560 V, T_A = 125°C				500	µA
Breakdown Voltage	BV_{DSS}	Device in Latched Shutdown I_C = 4 mA, I_D = 500 µA, T_A = 25°C		700			V
Rise Time	t_r	Measured With Figure 8 Schematic			100		ns
Fall Time	t_f	Measured With Figure 8 Schematic			50		ns
SUPPLY							
DRAIN Supply Voltage		See Note 2		36			V
Shunt Regulator Voltage	$V_{C(SHUNT)}$	I_C = 4 mA		5.5	5.8	6.1	V
Shunt Regulator Temperature Drift					±50		ppm/°C
CONTROL Supply/ Discharge Current	I_{CD1}	Output MOSFET enabled	TOP200/1/2	0.6	1.2	1.6	mA
			TOP203/4/14	0.7	1.4	1.8	
	I_{CD2}	Output MOSFET Disabled		0.5	0.8	1.1	

NOTES:

1. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

2. It is possible to start up and operate *TOPSwitch* at DRAIN voltages well below 36 V. However, the CONTROL pin charging current is reduced, which affects start-up time and auto-restart frequency and duty cycle. Refer to the characteristic graph on CONTROL pin charge current (I_C) vs. DRAIN voltage for low voltage operation characteristics.

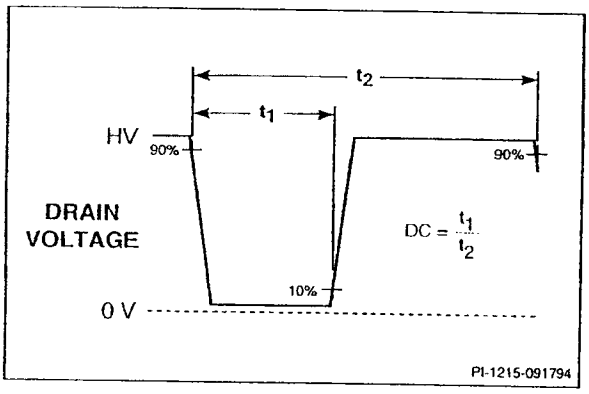


Figure 12. TOPSwitch Duty Cycle Measurement.

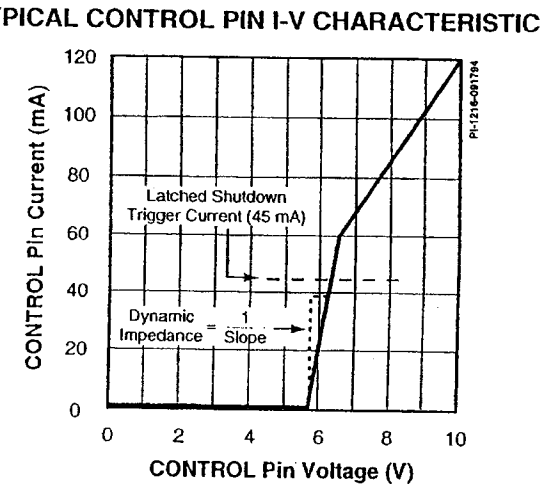


Figure 13. TOPSwitch CONTROL Pin I-V Characteristic.

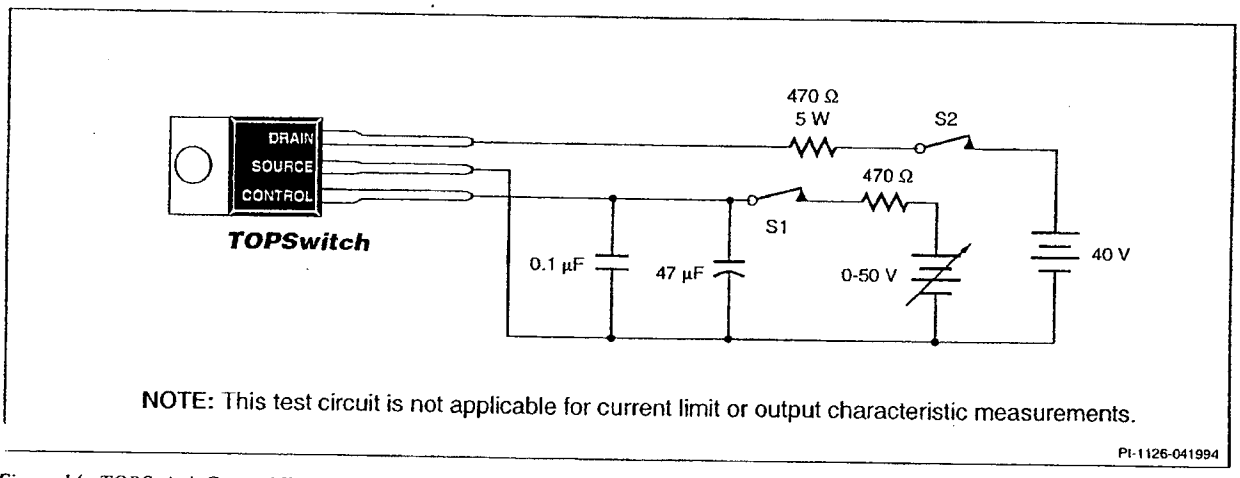


Figure 14. TOPSwitch General Test Circuit.

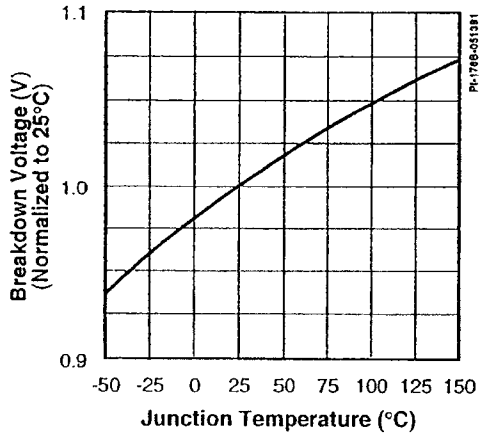
BENCH TEST PRECAUTIONS FOR EVALUATION OF ELECTRICAL CHARACTERISTICS

The following precautions should be followed when testing *TOPSwitch* by itself outside of a power supply. The schematic shown in Figure 14 is suggested for laboratory testing of *TOPSwitch*.

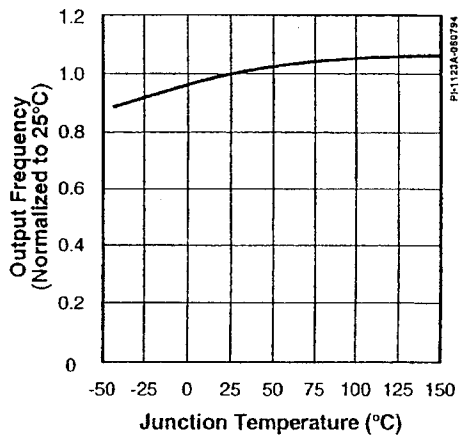
When the DRAIN supply is turned on, the part will be in the auto-restart mode. The control pin voltage will be oscillating at a low frequency from 4.7 to 5.7 V and the DRAIN is turned on every eighth cycle of the CONTROL pin oscillation. If the CONTROL pin power supply is turned on while in this auto-restart mode, there is only a 12.5% chance that the control pin oscillation will be in the correct state (DRAIN active state) so that the continuous DRAIN voltage waveform may be observed. It is recommended that the V_C power supply be turned on first and the DRAIN power supply second if continuous drain voltage waveforms are to be observed. The 12.5% chance of being in the correct state is due to the 8:1 counter.

Typical Performance Characteristics

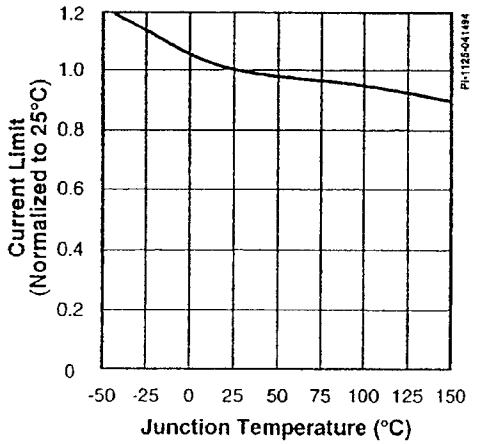
BREAKDOWN vs. TEMPERATURE



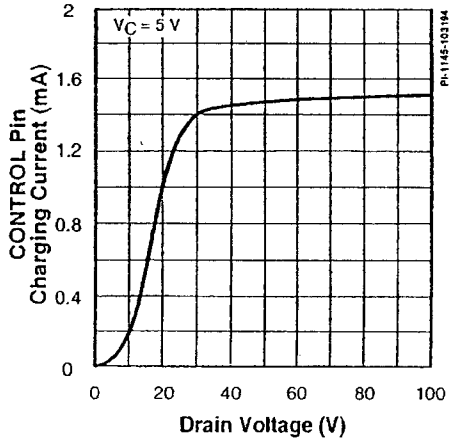
FREQUENCY vs. TEMPERATURE



CURRENT LIMIT vs. TEMPERATURE

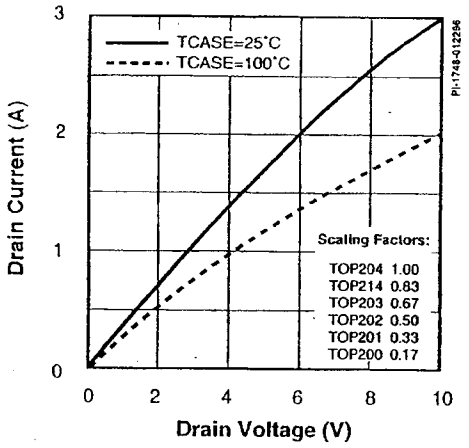


I_C vs. DRAIN VOLTAGE

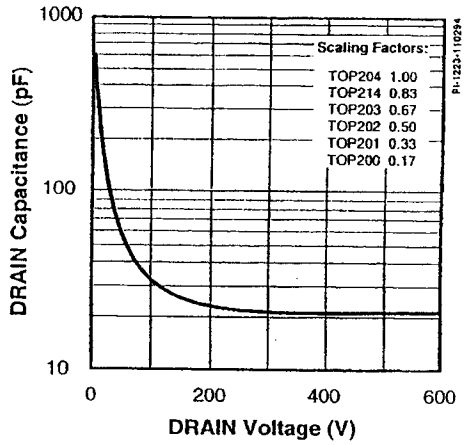


Typical Performance Characteristics (cont.)

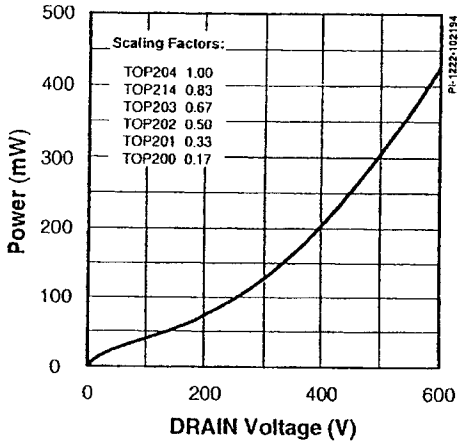
OUTPUT CHARACTERISTICS



C_{OSS} vs. DRAIN VOLTAGE



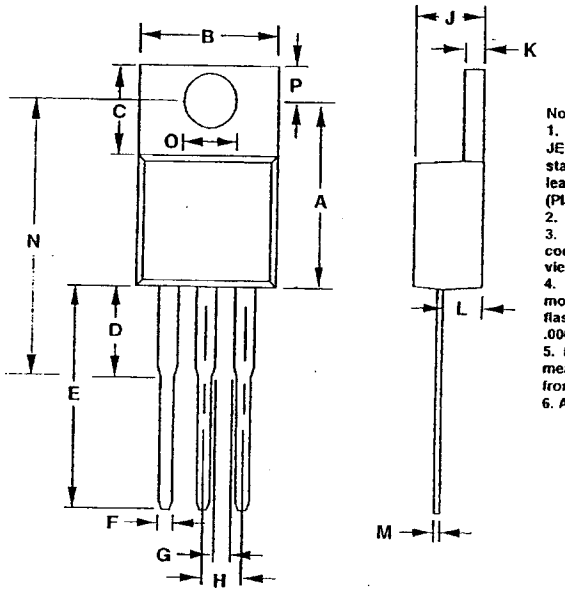
DRAIN CAPACITANCE POWER



Y03A — Plastic TO-220/3

DIM	inches	mm
A	.460-.480	11.68-12.19
B	.400-.415	10.16-10.54
C	.236-.260	5.99-6.60
D	.240 - REF.	6.10 - REF.
E	.520-.560	13.21-14.22
F	.028-.038	.71-.97
G	.045-.055	1.14-1.40
H	.090-.110	2.29-2.79
J	.165-.185	4.19-4.70
K	.045-.055	1.14-1.40
L	.095-.115	2.41-2.92
M	.015-.020	.38-.51
N	.705-.715	17.91-18.16
O	.146-.156	3.71-3.96
P	.103-.113	2.62-2.87

* LEADS AND TAB ARE SOLDER PLATED



Notes:
1. Package dimensions conform to JEDEC specification TO-220 AB for standard flange mounted, peripheral lead package; .100 inch lead spacing (Plastic) 3 leads (issue J, March 1987)
2. Controlling dimensions are inches.
3. Pin numbers start with Pin 1, and continue from left to right when viewed from the top.
4. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15 mm) on any side.
5. Position of terminals to be measured at a position .25 (6.35 mm) from the body.
6. All terminals are solder plated.

PI-1848-050696

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EXHIBIT C

TOP221-227

TOPSwitch®-II Family

Three-terminal Off-line PWM Switch

POWER INTEGRATIONS, INC.

Product Highlights

- Lowest cost, lowest component count switcher solution
- Cost competitive with linears above 5W
- Very low AC/DC losses – up to 90% efficiency
- Built-in Auto-restart and Current limiting
- Latching Thermal shutdown for system level protection
- Implements Flyback, Forward, Boost or Buck topology
- Works with primary or opto feedback
- Stable in discontinuous or continuous conduction mode
- Source connected tab for low EMI
- Circuit simplicity and Design Tools reduce time to market

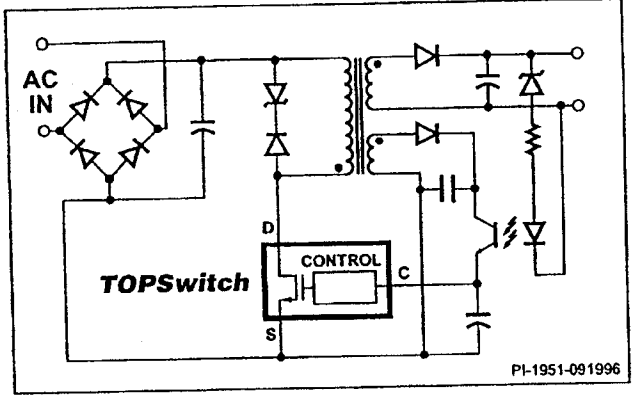

Figure 1. Typical Flyback Application.

Description

The second generation *TOPSwitch-II* family is more cost effective and provides several enhancements over the first generation *TOPSwitch* family. The *TOPSwitch-II* family extends the power range from 100W to 150W for 100/115/230 VAC input and from 50W to 90W for 85-265 VAC universal input. This brings *TOPSwitch* technology advantages to many new applications, i.e. TV, Monitor, Audio amplifiers, etc. Many significant circuit enhancements that reduce the sensitivity to board layout and line transients now make the design even easier. The standard 8L PDIP package option reduces cost in lower power, high efficiency applications. The internal lead frame of this package uses six of its pins to transfer heat from the chip directly to the board, eliminating the cost of a heat sink. *TOPSwitch* incorporates all functions necessary for a switched mode control system into a three terminal monolithic IC: power MOSFET, PWM controller, high voltage start up circuit, loop compensation and fault protection circuitry.

OUTPUT POWER TABLE

TO-220 (Y) Package[1]			8L PDIP (P) or 8L SMD (G) Package[2]		
PART ORDER NUMBER	Single Voltage Input[3] 100/115/230 VAC ±15% P_{MAX}[4,6]	Wide Range Input 85 to 265 VAC P_{MAX}[4,6]	PART ORDER NUMBER	Single Voltage Input[3] 100/115/230 VAC ±15% P_{MAX}[5,6]	Wide Range Input 85 to 265 VAC P_{MAX}[5,6]
TOP221Y	12 W	7 W	TOP221P or TOP221G	9 W	6 W
TOP222Y	25 W	15 W	TOP222P or TOP222G	15 W	10 W
TOP223Y	50 W	30 W	TOP223P or TOP223G	25 W	15 W
TOP224Y	75 W	45 W	TOP224P or TOP224G	30 W	20 W
TOP225Y	100 W	60 W			
TOP226Y	125 W	75 W			
TOP227Y	150 W	90 W			

Notes: 1. Package outline: TO-220/3 2. Package Outline: DIP-8 or SMD-8 3. 100/115 VAC with doubler input 4. Assumes appropriate heat sinking to keep the maximum *TOPSwitch* junction temperature below 100 °C. 5. Soldered to 1 sq. in.(6.45 cm^2), 2 oz. copper clad (610 gm/m^2) 6. P_{MAX} is the maximum practical continuous power output level for conditions shown. The continuous power capability in a given application depends on thermal environment, transformer design, efficiency required, minimum specified input voltage, input storage capacitance, etc. 7. Refer to key application considerations section when using *TOPSwitch-II* in an existing *TOPSwitch* design.

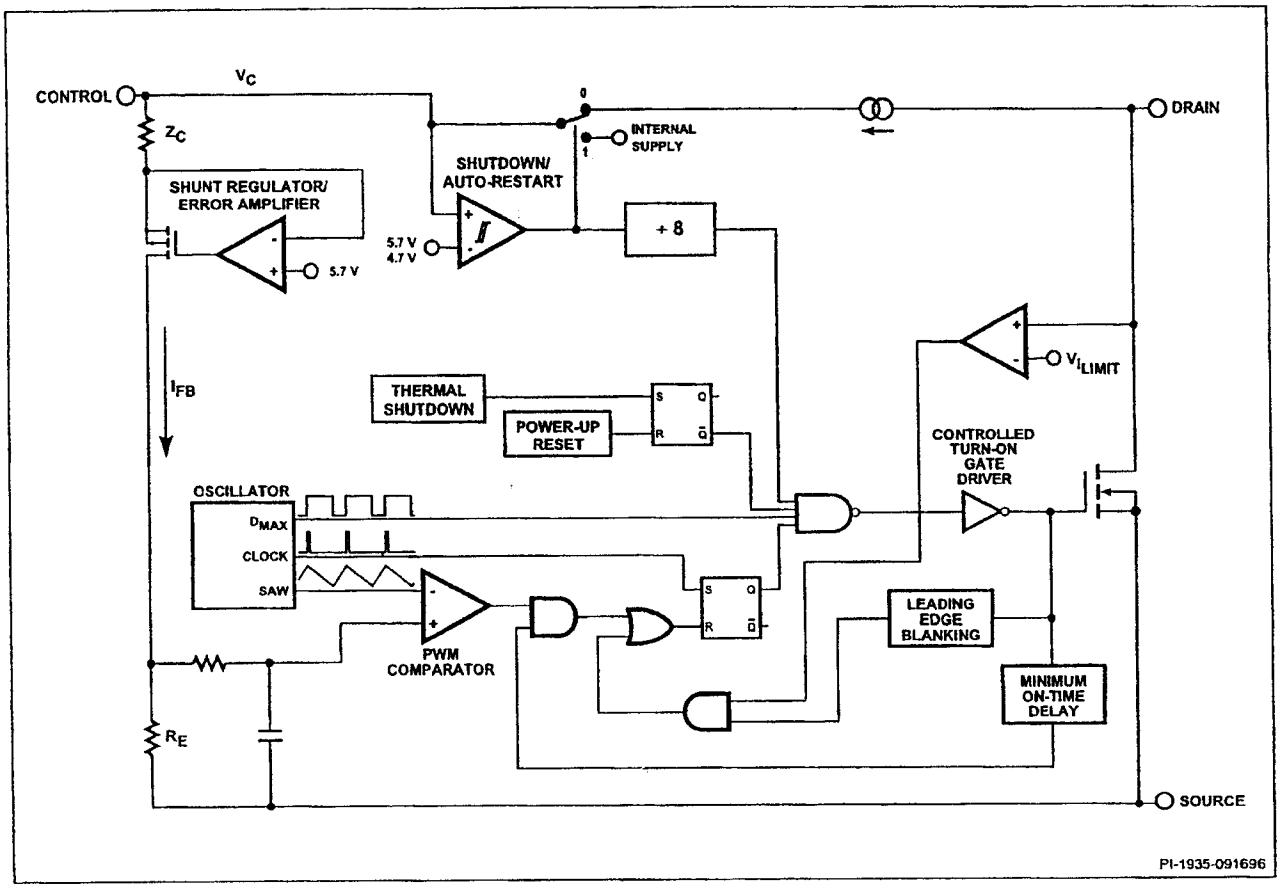

Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN Pin:
Output MOSFET drain connection. Provides internal bias current during start-up operation via an internal switched high-voltage current source. Internal current sense point.

CONTROL Pin:
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. It is also used as the connection point for the supply bypass and auto-restart/ compensation capacitor.

SOURCE Pin:
Y package – Output MOSFET source connection for high voltage power return. Primary side circuit common and reference point.

P and G package – Primary side control circuit common and reference point.

SOURCE (HV RTN) Pin: (P and G package only)
Output MOSFET source connection for high voltage power return.

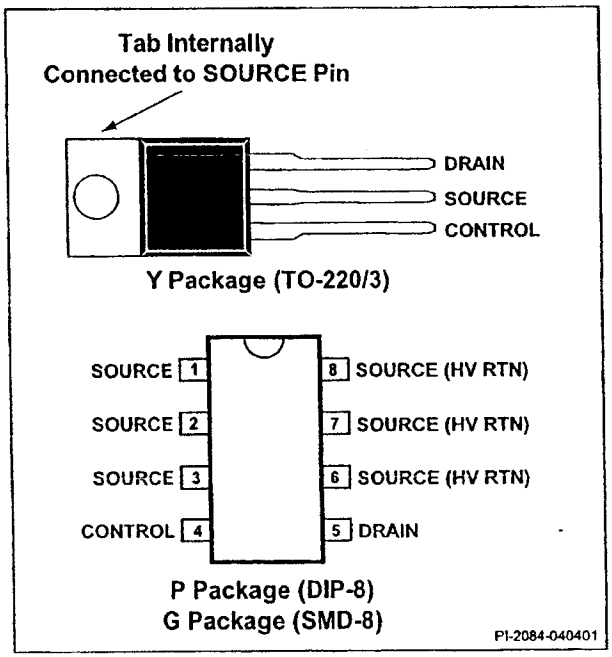

Figure 3. Pin Configuration.

TOPSwitch-II Family Functional Description

TOPSwitch is a self biased and protected linear control current-to-duty cycle converter with an open drain output. High efficiency is achieved through the use of CMOS and integration of the maximum number of functions possible. CMOS process significantly reduces bias currents as compared to bipolar or discrete solutions. Integration eliminates external power resistors used for current sensing and/or supplying initial start-up bias current.

During normal operation, the duty cycle of the internal output MOSFET decreases linearly with increasing CONTROL pin current as shown in Figure 4. To implement all the required control, bias, and protection functions, the DRAIN and CONTROL pins each perform several functions as described below. Refer to Figure 2 for a block diagram and to Figure 6 for timing and voltage waveforms of the *TOPSwitch* integrated circuit.

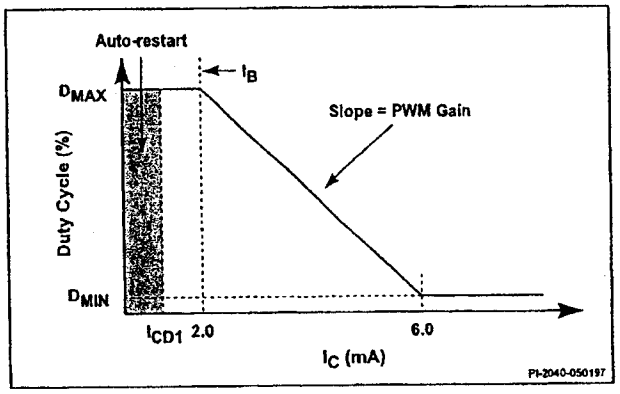

Figure 4. Relationship of Duty Cycle to CONTROL Pin Current.

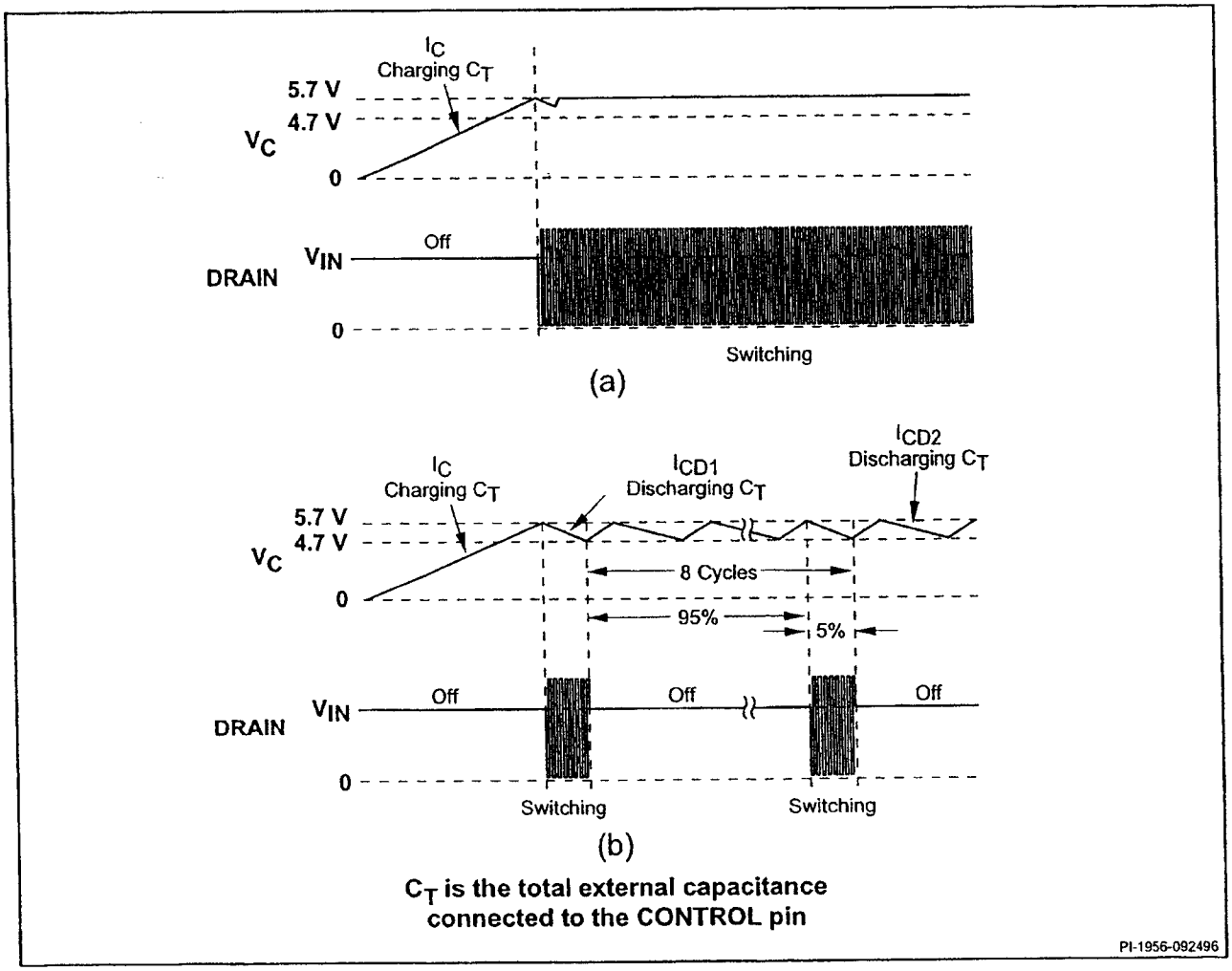

Figure 5. Start-up Waveforms for (a) Normal Operation and (b) Auto-restart.

TOPSwitch-II Family Functional Description (cont.)

Control Voltage Supply

CONTROL pin voltage V_C is the supply or bias voltage for the controller and driver circuitry. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the gate drive current. The total amount of capacitance connected to this pin (C_T) also sets the auto-restart timing as well as control loop compensation. V_C is regulated in either of two modes of operation. Hysteretic regulation is used for initial start-up and overload operation. Shunt regulation is used to separate the duty cycle error signal from the control circuit supply current. During start-up, CONTROL pin current is supplied from a high-voltage switched current source connected internally between the DRAIN and CONTROL pins. The current source provides sufficient current to supply the control circuitry as well as charge the total external capacitance (C_T).

The first time V_C reaches the upper threshold, the high-voltage current source is turned off and the PWM modulator and output transistor are activated, as shown in Figure 5(a). During normal operation (when the output voltage is regulated) feedback control current supplies the V_C supply current. The shunt regulator keeps V_C at typically 5.7 V by shunting CONTROL pin feedback current exceeding the required DC supply current through the PWM error signal sense resistor R_E. The low dynamic impedance of this pin (Z_C) sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance of the CONTROL pin together with the external resistance and capacitance determines the control loop compensation of the power system.

If the CONTROL pin total external capacitance (C_T) should discharge to the lower threshold, the output MOSFET is turned off and the control circuit is placed in a low-current standby mode. The high-voltage current source turns on and charges the external capacitance again. Charging current is shown with a negative polarity and discharging current is shown with a positive polarity in Figure 6. The hysteretic auto-restart comparator keeps V_C within a window of typically 4.7 to 5.7 V by turning the high-voltage current source on and off as shown in Figure 5(b). The auto-restart circuit has a divide-by-8 counter which prevents the output MOSFET from turning on again until eight discharge-charge cycles have elapsed. The counter effectively limits *TOPSwitch* power dissipation by reducing the auto-restart duty cycle to typically 5%. Auto-restart continues to cycle until output voltage regulation is again achieved.

Bandgap Reference

All critical *TOPSwitch* internal voltages are derived from a temperature-compensated bandgap reference. This reference is also used to generate a temperature-compensated current source which is trimmed to accurately set the oscillator frequency and MOSFET gate drive current.

Oscillator

The internal oscillator linearly charges and discharges the internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle. The nominal frequency of 100 kHz was chosen to minimize EMI and maximize efficiency in power supply applications. Trimming of the current reference improves the frequency accuracy.

Pulse Width Modulator

The pulse width modulator implements a voltage-mode control loop by driving the output MOSFET with a duty cycle inversely proportional to the current into the CONTROL pin which generates a voltage error signal across R_E. The error signal across R_E is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise. The filtered error signal is compared with the internal oscillator sawtooth waveform to generate the duty cycle waveform. As the control current increases, the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the output MOSFET. The pulse width modulator resets the latch, turning off the output MOSFET. The maximum duty cycle is set by the symmetry of the internal oscillator. The modulator has a minimum ON-time to keep the current consumption of the *TOPSwitch* independent of the error signal. Note that a minimum current must be driven into the CONTROL pin before the duty cycle begins to change.

Gate Driver

The gate driver is designed to turn the output MOSFET on at a controlled rate to minimize common-mode EMI. The gate drive current is trimmed for improved accuracy.

Error Amplifier

The shunt regulator can also perform the function of an error amplifier in primary feedback applications. The shunt regulator voltage is accurately derived from the temperature compensated bandgap reference. The gain of the error amplifier is set by the CONTROL pin dynamic impedance. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and flows through R_E as a voltage error signal.

Cycle-By-Cycle Current Limit

The cycle by cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET ON-state drain-source voltage, $V_{DS(ON)}$ with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature